300 GHz broadband power amplifier with 508 GHz gain-bandwidth product and 8 dBm output power

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***Abstract* — This paper presents a broadband H-band (220 - 325 GHz) power amplifier in a 35 nm InGaAs-based metamorphic high electron mobility transistor technology. The amplifier is realized as a submillimeter-wave monolithic integrated circuit (S-MMIC) and is designed to drive a high power amplifier in a multi-gigabit communication system. The five-stage amplifier S-MMIC based on common-source gain cells was realized and measured on-wafer with a maximum gain of 23 dB at 285 GHz. The lower and higher cutoff frequency is 278 and 335 GHz, respectively, with a gain variation of around 4 dB. The amplifier has four parallel transistors in the last two stages and provides a saturated output power of 8 dBm at 300 GHz. A gain-bandwidth product (GBW) of 508 GHz could be achieved.**

***Keywords* — H-band, power amplifier (PA), metamorphic high electron mobility transistor (mHEMT), submillimeter-wave monolithic integrated circuit (S-MMIC).**

I. Introduction

Power amplifiers (PAs) are important for nearly any radio frequency (RF) system. Mainly in the last stage of a transmitter chain a PA is placed to provide enough output power. Whether radar or communication is the application, the output power has a decisive influence on the performance of the system. A high output power can compensate a small antenna gain or a higher distance with adverse atmospheric effects that reduce the power density. Finally, the solid state PA (SSPA) can also be used a driver stage, e.g. to drive a traveling wave tube amplifier (TWTA) which typically requires high input power levels exceeding 10 dBm [1].

In this paper we present a SSPA operating at a center frequency of 300 GHz for high-speed wireless communication. The chip is designed in a 35 nm InGaAs mHEMT technology. The electrical parameters f_t and f_{max} are more than 500 GHz and 1000 GHz, respectively, for this technology [2]. The bandwidth should exceed 50 GHz to support the target baud rate of at least 25 Gbaud in the communication applications. The linear output power is of highest importance in a communication system to be able to send higher order modulation formats to increase the spectral efficiency. The 1-dB compression point (P_{1dB}) should be as high as possible, because the amplifier has to operate in a certain amount of back-off to transmit complex modulated signals such as quadrature amplitude modulation (QAM). The high gain of the power amplifier of 20 dB is required because the upconverter in a 300 GHz communication system typically provides around -16 dBm of output power [3].

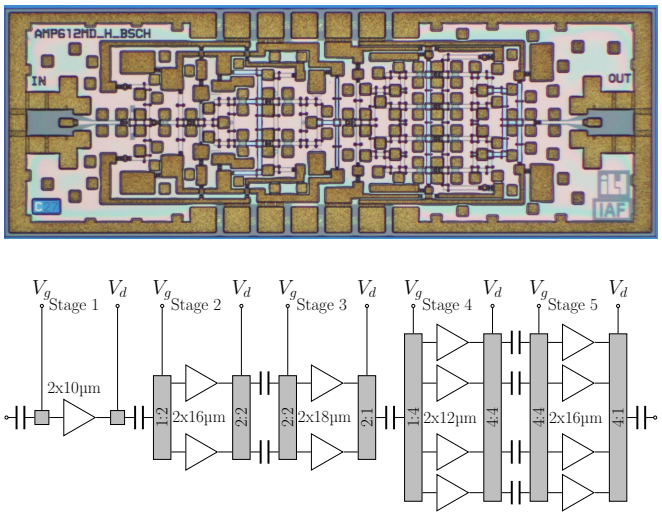

Fig. 1. Chip photograph and block diagram of the five-stage broadband power amplifier. Chip size is 2 mm x 0.75 mm.

II. Circuit Design

Fig. 1 shows the chip photograph and a block diagram of the realized broadband power amplifier MMIC. A grounded coplanar waveguide (GCPW) environment with a ground to ground spacing of 14 µm has been used for the reactive (input, output and interstage) impedance matching networks. The RF input and output pads are shielded with vias for an accurate calibration in the small-signal measurement [4]. The amplifier consists of five gain stages with four parallel transistors in the last two stages. The design was built largely symmetric with DC pads in the north and south of the chip. It is not necessary to connect both, because there is a connection through the parallel stages from north to south, but this redundant feature was included for ease of on-chip measurement and packaging as well as increased symmetry. All transistors are in common-source configuration and operating in class A mode. For input and output matching, transmission lines and series capacitors were used. All biasing networks are included in the matching and consist of an RF shorted stub line followed by a metal insulator metal (MIM) capacitor to ground. The series resistors in the gate biasing are for stability improvement to suppress low frequency oscillations. In the drain bias network a resistor and MIM-capacitor parallel to ground are employed to avoid losses. In case of in-band-oscillation a resistor with a parallel capacitor was placed in the signal path in front of the first gate terminal. These layout features result in an over-all

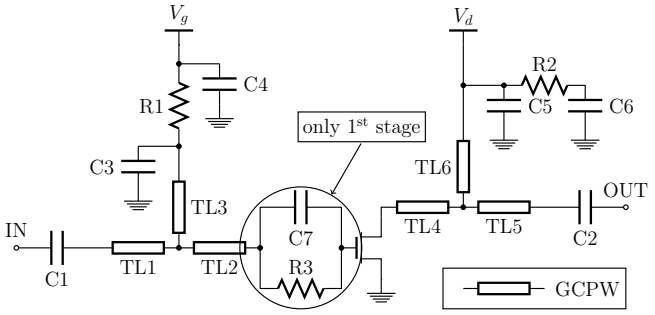

Fig. 2. Schematic diagram of a single common source amplifier stage.

chip size of $2 \times 0.75\,\mathrm{mm}^2$.

A single stage gain cell with matching and bias networks is shown in Fig. 2. The series capacitors C1 and C2 are decoupling the RF input and output from gate and drain bias. The input and output of the power amplifier is matched to $50\,\Omega$. Between the gain stages a non $50\,\Omega$ environment is chosen to reduce the matching losses. TL1 to TL3 form the input matching network and provide the gate bias. The gate bias path is decoupled from RF path with C3, C4 and R1. The resistor R1 improves the stability especially at low frequencies. TL4 to TL6 form the output matching network and provide the drain bias with C5 for RF decoupling. C6 and R2 are implemented for low-frequency stability. The utilized transistors have two gate fingers with an increasing gate width through the stages.

Fig. 1 shows a block diagram of the five-stage power amplifier with the gate width of each gain stage. The gate widths were chosen in a way to avoid compression in the first stages. The amplifier input is a single stage followed by two times two parallel transistors. The last two stages employ four parallel transistors to increase the output power. Compact power combiners and dividers are placed in order to parallelize the branches and to save space in comparison to standard Wilkinson combiners. The interstage matching structures between stages two to five also provides the biasing. The chosen topology for the matching between stages is not fully symmetric but it has less losses than the alternative of combing and splitting networks. For stability consideration the k-factor is necessary but is not sufficient, because internal oscillations between the stages and odd-mode oscillations cannot be detected. For that purpose the reflection coefficient method was applied for different input and output impedances at all active/passive interfaces. The amplifier circuit was simulated in Keysight Advanced Design System (ADS) using compact transistor models described in [5] and [6]. In addition, a 3D electromagnetic (EM) field simulation was performed to investigate the influence of the complex passive structures such as the 4:1 reduced Wilkinson combiner in the last stage. The 3D EM simulation was performed using CST Microwave Studio.

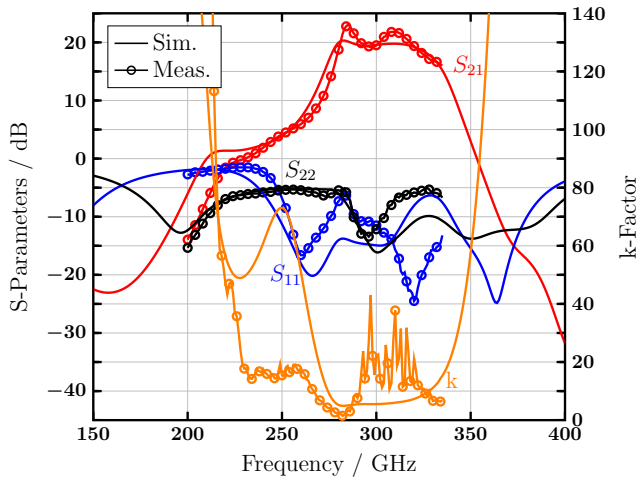

Fig. 3. On-wafer measured and simulated S-parameters and k-factor of five-stage 35-nm mHEMT amplifier S-MMIC from 200 to 335 GHz.

III. Measurement

A. Small Signal Measurement

The chip was characterized in an on-wafer measurement setup. The measured S-parameters are shown in Fig. 3 with a small signal gain of more than 19 dB in the frequency range of 278 to 335 GHz which corresponds to a bandwidth of 57 GHz. The maximum gain of 23 dB is located at 285 GHz. The bias condition of the small signal measurement was $V_d = 0.8\mathrm{V}$ and $V_g = 0.13\mathrm{V}$. For this bias point the total current draw by the power amplifier is $I_d = 144\,\mathrm{mA}$ which results in a current density of each transistor of $I_d = 380\,\mathrm{mA\,mm^{-1}}$. The magnitudes of the measured input and output reflection parameter for the operation bandwidth are below $-6\,\mathrm{dB}$ and $-5\,\mathrm{dB}$, respectively. The isolation is in the on-wafer measurement setup below $-35\,\mathrm{dB}$. The k-factor derived from the measured S-parameters has the lowest value of 1.5 at 282 GHz in the operation band. From DC to 200 GHz the value of k is beyond 1 according to simulation.

B. Power Measurement

An on-wafer scalar power measurement was performed with a bias setting $V_d = 1\mathrm{V}$ and $V_g = 0.12\mathrm{V}$. The current density of the transistors was the same as in the small signal measurement. Fig. 4 shows the simulated and measured gain, output power and power added efficiency (PAE) in relation to the input power. The measured transducer gain is above the measured S_{21}, because of the higher drain voltage. A $\mathrm{P_{1dB,in}}$ can only be estimated at around -16 dBm, because of the power range limitation. In simulation the $\mathrm{P_{1dB,in}}$ is located at -14 dBm of input power at a frequency of 300 GHz. The saturated output power of 6.9 dBm can be observed for an input power of $-4\,\mathrm{dBm}$ at 300 GHz for this bias point. At this point the PAE is 3.06% and the total DC power consumption of the MMIC is $144\,\mathrm{mW}$. Fig. 5 shows the simulated and measured output power against frequency for an input power of $-13\,\mathrm{dBm}$ and $-4\,\mathrm{dBm}$. The amplifier chip was measured in different bias points.

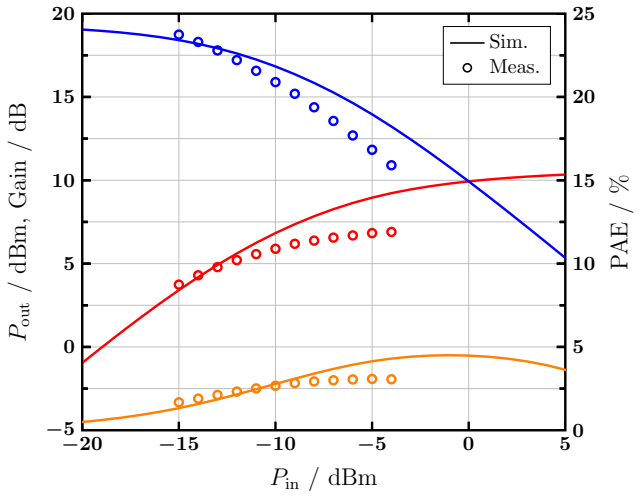

Fig. 4. On-wafer measured large-signal performance of the power amplifier for 300 GHz with $V_{\mathrm{d}} = 1.0\,\mathrm{V}$, $V_{\mathrm{g}} = 0.12\,\mathrm{V}$ and $I_{\mathrm{d}} = 144\,\mathrm{mA}$.

Fig. 6 shows the output power for different drain current densities by applying a drain voltage of 1.2 V at 300 GHz. Here, the maximum saturated output power of 8 dBm can be observe for a drain current density of $430\,\mathrm{mA\,mm^{-1}}$. The chip has in this operation point a total DC power consumption of 202 mW with a PAE of 2.97%. Fig. 7 shows the saturated output power by varying the drain voltage from 0.6 to 1.2 V with a constant drain current density of $380\,\mathrm{mA\,mm^{-1}}$.

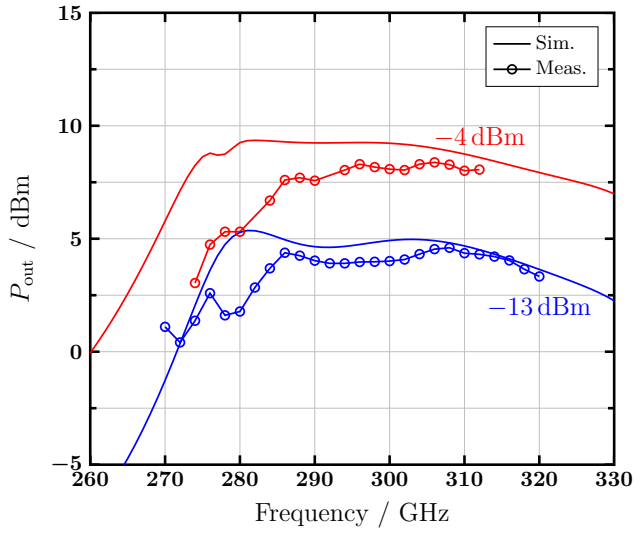

Fig. 5. Simulated and on-wafer measured output power as a function of frequency for -13 dBm and -4 dBm of input power.

IV. State of the Art

In Table 1 a comparison of reported power amplifier around 300 GHz is included. The maximum output power is achieved in [7] with a narrow band design and a gain of 13.4 dB. Amplifier with a higher GBW reaches only up to 10 dBm of output power. In principle the InP technology allows high supply voltages up to 4.5 V in comparison to

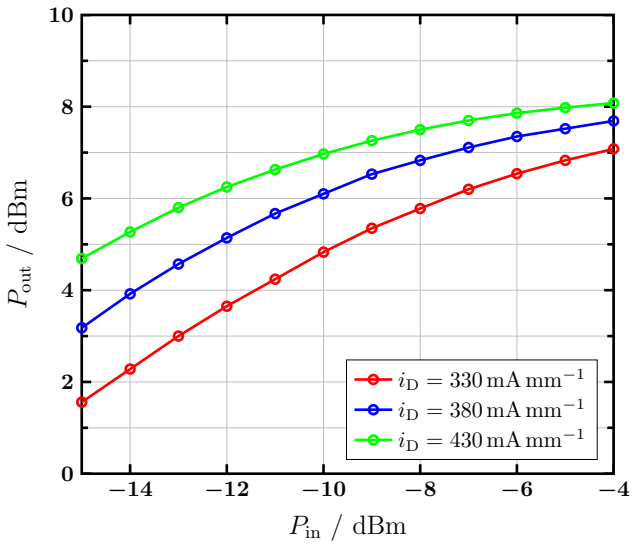

Fig. 6. On-wafer measured output power as a function of input power for different drain current densities with $V_{\mathrm{d}} = 1.2\,\mathrm{V}$ at 300 GHz.

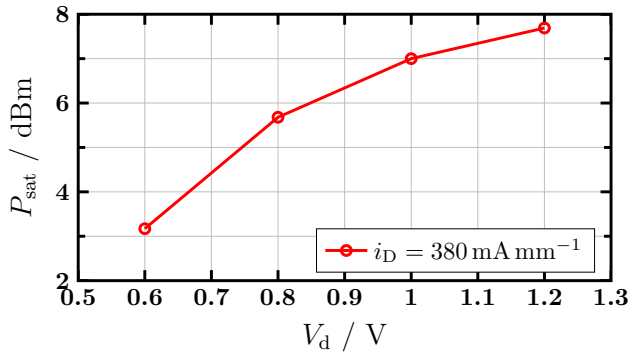

Fig. 7. On-wafer measured saturated output power as a function of drain voltage for a drain current densities of $380\,\mathrm{mA\,mm^{-1}}$ at 300 GHz.

1.5 V in this paper and for that more ouput power can be achieved. On the other hand the MMICs on a GaAs substrate are more broadband. This results in a higher GBW. Compared to amplifiers in the same technology we can achieve the highest output power and a second best GBW reported in this frequency range. The amplifier in [8] has the highest GBW, because of its huge bandwidth of 128 GHz. For a direct comparison a Figure of Merit (FoM) is defined as:

$$\mathrm{FoM} = \frac{\mathrm{Gain}\cdot\mathrm{BW}}{\mathrm{GHz}} \cdot \frac{P_{\mathrm{sat}}}{\mathrm{mW}} \cdot \frac{f_c}{f_{\mathrm{max}}} \Big/ \frac{P_{\mathrm{DC}}}{\mathrm{mW}} \tag{1}$$

consisting of the gain-bandwidth product and the saturated output power related to the fraction of the center frequency and the technology's maximum oscillation frequency. Finally, the total DC power consumption is taken into account, since efficiency is an important criteria for power amplifiers. Some of the referenced amplifiers exceed this work in individual characteristics. But in the overall performance, which is represented by the FoM, this work presents the best FoM-value of the reported amplifiers.

Table 1. State-of-the-Art power amplifiers around 300 GHz (f_c:center frequency, P_{DC}: DC power consumption,*extracted from graphic, **module performance)

Technology	f_{max} / THz	f_c / GHz	S_{21} / dB	P_{sat} / dBm	BW / GHz	GBW / GHz	P_{DC} / mW	FoM	Reference
250 nm InP HBT	0.859	301	13.4	13.5	15*	70	169	3.2	[7]
35 nm InGaAs mHEMT	1	240	16	4.8**	128	808	129	4.5	[8]
250 nm InP HBT	0.859	300	23.5	10	17.5	262	848	1.1	[9]
130 nm InP HBT	1.15	325	16.6	11.3	9	60	1120	0.2	[10]
50 nm InP HEMT	1.2	340	11.5	10	10	37	294.8	0.4	[11]**
250 nm InP HBT	0.859	300	21.8	9.8	40	492	720	2.3	[12]
35 nm InGaAs mHEMT	1	240	12.7	6.2	120	518	-	-	[13]
35 nm InGaAs mHEMT	1	300	19	8	57	508	202	4.8	**this work**

V. Conclusion

A H-band five-stage broadband power amplifier for high data rate communication applications has been reported. The design utilizes InGaAs mHEMT based gain cells in a common source configuration. The power amplifier has a center frequency of 300 GHz with a small signal gain of 19 dB with 4 dB of gain variation in the operation band. The maximum measured saturated output power is 8 dBm with a corresponding PAE of 2.97% at 300 GHz. The amplifier shows the best reported combination of gain-bandwidth product, output power and efficiency in a 300 GHz power amplifier. This amplifier will be integrated with frequency-converting stages to form a complete analog transmit frontend for ultra-wideband terahertz communication.

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