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Institute of
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2020 Seminar on Selected Topics on Power and Microwave Electronics

SEMINAR PROCEEDINGS

Selected Topics on Power and Microwave Electronics

- **Substrate integrated waveguides** for millimeter waves electronics
- **Measurement methods and techniques** in power electronics
- **Analog Pre-Distortion** for millimeter waves amplifiers
- **Characterisation and modelling** of power semiconductor devices
- **Bondwire impedance** compensation for radio frequency chip interconnects

- **Scientific writing** and presentation of a conference paper
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- **Summer term 2020, 6 ECTS**

Contact

Institute of Robust Power Semiconductor Systems
University of Stuttgart
Pfaffenwaldring 47
70569 Stuttgart, Germany

www.ilh.uni-stuttgart.de

Prof. Dr.-Ing. Ingmar Kallfass
ingmar.kallfass@ilh.uni-stuttgart.de

M.Sc. Lixi Yan
lixi.yan@ilh.uni-stuttgart.de

Bond-Wire Impedance Compensation for Millimeter-Wave Chip Interconnects

Max Lippoldt
University of Stuttgart, Stuttgart, Germany
max.lippoldt@gmx.de

***Abstract*—This paper presents and compares different techniques that enable the use of bond-wire connections at millimeter-wave frequencies. Starting from a simple equivalent circuit representation of the bond-wire, basic techniques of how to increase its operating frequency range are discussed. Also, a rule of thumb is presented to estimate up to which frequency limit an uncompensated bond-wire of a certain length can be used. To increase the operating frequency range beyond this limit, compensation of the bond-wire inductance is required. Based on a literature review, state-of-the-art compensation techniques are presented: A series resonance approach, two simple low-pass approaches, a multi-stage LC low-pass approach, an approach based on a quarter-wavelength transformer, and an approach that treats the interconnect as a half-wavelength long transmission line. The advantages and disadvantages of each technique are discussed as well as practical limitations. Each approach is analyzed in terms of required on-chip area, operating bandwidth, insertion loss, and its robustness against fabrication tolerances. Also, a comparison of all presented techniques is made.**

***Index Terms*—MMIC, millimeter-wave, wire bonding**

I. Introduction

WIRE bonding is a standard technology to connect an integrated circuit (IC) to the outside world, for example to a printed circuit board (PCB). It uses thin metal wires to establish a connection between an on-chip pad and its off-chip counterpart. At low frequencies, this connection is quite ideal, apart from its limited maximum current. At higher frequencies, however, the inductance of the bond-wire starts to degrade the performance of the interconnect as it introduces an impedance mismatch and thereby leads to reflection losses. Thus it appears that it is impossible to use a simple bond-wire at millimeter-wave frequencies (defined as 30 GHz – 300 GHz).

Still, it would be desirable to use wire bonding at millimeter-waves because it is a well-established technology and thus cheap and broadly available. For that reason, a variety of techniques have been developed that allow to extend the useable frequency range of wire bonding into the millimeter-wave range, even beyond 100 GHz.

This paper summarizes the state of the art in bond-wire compensation techniques. It focuses solely on wire bonding because this technology is broadly available and cheap. Other approaches such as flip-chip and ribbon bonds are therefore beyond the scope of this paper.

The paper is organized as follows: Chapter 2 introduces the equivalent circuit of a bond-wire, shows techniques to reduce its inductance, and presents a rule-of-thumb for up to which frequency an uncompensated wire can be used. Chapter 3 discusses several compensation techniques and compares them regarding their bandwidth, on-chip area consumption and robustness against fabrication tolerances.

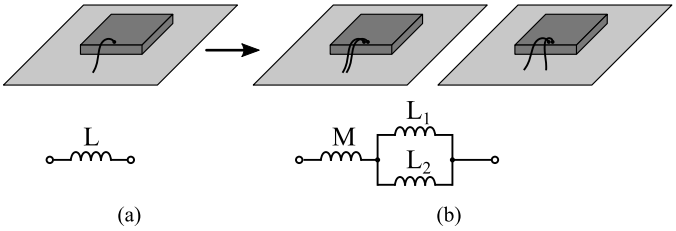

Fig. 1. (a) Equivalent circuit of a bond-wire connection. (b) Double wires or so-called V bonds can be used to decrease the effective inductance.

II. Uncompensated Bond-Wire

As stated above, the bond-wire can be considered as a lumped series inductance (see Fig. 1(a)). This approximation is valid at frequencies where the bond-wire length is below a tenth of the wavelength, e.g. up to 150 GHz for a wire of 0.2 mm length. The resistive losses in the wire as well as the parallel capacitance to ground are negligible because of its short length and width, respectively. However, if the bond-wire length is above a tenth of the wavelength (by increasing either the frequency or the wire length), it needs to be considered as a transmission line section. For all but one compensation approach presented in this paper, it is sufficient to view the bond-wire as a series inductance as its length is kept as short as technologically possible.

The inductance of the bond-wire can be approximated by the well-known inductor formula [1]

$$L = \frac{\mu_0}{2\pi}\, l\, \left(\ln\left(\frac{2l}{r}\right) - 0.75\right) \tag{1}$$

where L is the inductance, l is the bond-wire length, r is the bond-wire radius, and μ_0 is the free-space permittivity.

According to [2], this formula exaggerates the bond-wire inductance by 10–50% but shall be used here as a rough estimate. If typical values are inserted into this equation, one obtains the rule of thumb of 1 nH per millimeter bond-wire length.

The input impedance seen from the PCB increases with frequency due to this series inductance. That leads to an impedance mismatch and thereby to reflection losses which

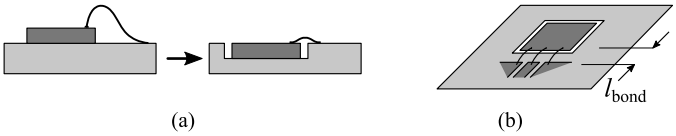

Fig. 2. (a) Wire length reduction by placing the chip in a cavity. (b) Definition of bond-wire length, coplanar configuration.

Fig. 3. Series resonance compensation: A series capacitance is used to cancel the imaginary part of the impedance at a single frequency [4].

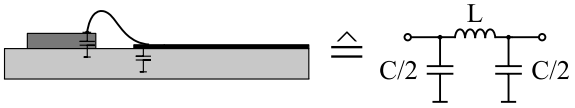

Fig. 4. CLC low-pass approach: Adding parallel capacitances to form an artificial transmission line/Butterworth low-pass [7].

increase with frequency. Thus the operating frequency range of this interconnect has an upper limit, typically defined by $|S_{11}| \leqslant -10$ dB (i.e. maximum 10% of the input signal power shall be reflected).

As a first approach to extend the frequency range, the effective inductance of the bond-wire connection can be decreased by placing two wires in parallel, as shown in Fig. 1(b). Because the two wires are in close proximity, a mutual inductance M is introduced [1] that again increases the effective inductance. This effect can be mitigated by using so-called V bonds (see Fig. 1(b)).

Another way to decrease the inductance of the bond-wire is to decrease the wire length. This can be achieved by placing the IC in a cavity in the PCB and by using wedge bonds, as shown in Fig. 2(a). With this technique, very short wire lengths in the range of 0.2 mm are achievable but come at the cost of very tight fabrication tolerances. Tight tolerances, in turn, lead to a decreased yield and thus will be avoided if possible.

Considering (1), it can be argued that using a thicker wire would also reduce its inductance. While this is true in principle, increasing the wire radius in turn limits the minimum wire length, which can be impractical because the inductance is more influenced by the length than by the radius. Thus the best approach seems to be to reduce the wire length as much as possible, and then to use the maximum available wire radius.

However, these techniques only reduce the inductance of the bond-wire and do not eliminate its effect completely. Thus the operating frequency range of the interconnect is limited. An estimate of the cutoff frequency has been presented for a coplanar waveguide-like interconnect [3]. In this configuration, the two outer wires connect the on-chip to the off-chip ground and the middle wire carries the signal (see Fig. 2(b)). The result obtained from a three-dimensional finite-element method simulation is that for $|S_{11}| \leqslant -10$ dB the length must satisfy:

$$l_{\text{bond}} \leqslant 0.033\,\lambda_0 \tag{2}$$

where l_{bond} is the bond-wire length and λ_0 is the free space wavelength.

For example, a bond-wire connection of 0.2 mm length can be used up to approximately 50 GHz. This means that for many practical applications, such as short-range communication at 60 GHz or automotive radar at 77 GHz, uncompensated bond-wires are no viable solution and that compensation techniques are needed.

III. Compensation Techniques

In this chapter, several techniques to compensate the bond-wire inductance are presented. Each approach is analyzed in terms of bandwidth, area consumption, insertion loss, and robustness against tolerances. At the end of this chapter, the different techniques are compared.

A. Series Resonance Compensation

The first approach to compensate the equivalent series inductance of the bond-wire is to add a series capacitance [4]–[6]. The resulting structure as well as its schematic representation is shown in Fig. 3. To compensate the inductive effect of the bond-wire, it is required that the reactances of both the bond-wire and the capacitance are equal, i.e.:

$$\omega L = \frac{1}{\omega C} \tag{3}$$

where L is the bond-wire inductance, C is the series capacitance, and $\omega = 2\pi f$ is the angular frequency.

As can be observed from (3), this compensation theoretically only works at a single frequency, which means that it is very narrowband. This also means that this approach is quite sensitive to fabrication tolerances. On the other hand, it offers a very low area consumption as well as very low insertion loss due to the minimal number of added components. Therefore, this approach is well-suited for narrowband applications, e.g. as an interconnect to an inherently narrowband patch antenna.

B. CLC Low-Pass

Another simple approach to compensate the equivalent series inductance of the bond-wire is to add parallel capacitances both on- and off-chip [7]–[9] (see Fig. 4). Together with the bond-wire inductance, a CLC-circuit is formed that can be seen as a short transmission line section with the impedance $Z = \sqrt{L/C}$. By choosing an appropriate value for the capacitances, this impedance can be made equal to the reference impedance (typically 50 Ohm) and thus no reflection losses occur. The capacitances can be realized as parallel plate capacitors between different metal layers, or as

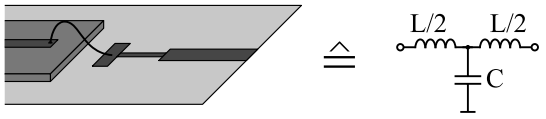

Fig. 5. LCL low-pass approach: Adding a parallel capacitance and a series inductance to form a T-section low-pass [10].

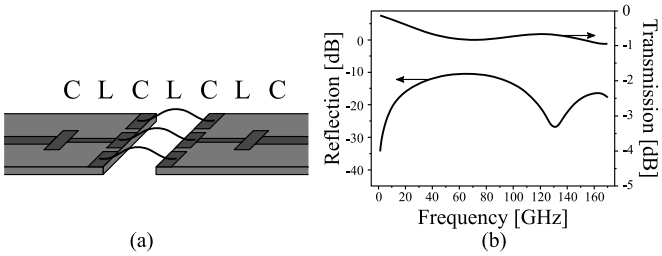

Fig. 6. (a) Layout of the seven-stage approach. (b) Measured S-parameters of the seven-stage approach. (both from [17])

open stubs. Advantageously, the required pads for the bonding process already inherently act as parallel capacitance, so that only minimal additional area is needed for this compensation approach.

Also, the insertion loss of this structure is very small because it only adds two parallel capacitances.

The operating frequency range of this compensation technique is limited by the fact that the CLC structure is not only an artificial transmission line, but also a Butterworth low-pass filter. Its cutoff frequency is given by:

$$f_{\text{cutoff}} = \frac{Z}{\pi L} \tag{4}$$

where Z is the reference impedance and L is the filter inductance, which in this case is equal to the bond-wire inductance.

Note that this cutoff frequency is defined by $|S_{21}| \geqslant -3$ dB (i.e. at least 50% of the input signal power are transmitted) and thus is always slightly higher than if it was defined in terms of $|S_{11}| \leqslant -10$ dB.

Still, this theoretical cutoff frequency can serve as a rough estimate. For example, a bond-wire of 0.2 mm length and 0.01 mm radius has an inductance of approximately 0.12 nH (from (1)), which leads to a cutoff frequency of about 130 GHz. Considering that the $|S_{11}| \leqslant -10$ dB cutoff frequency will be lower than that, it can be concluded that the CLC technique is applicable up to around 100 GHz at a wire length of 0.2 mm (versus up to 50 GHz without compensation, as mentioned above).

This approach is also quite robust against fabrication tolerances. A small deviation of the inductance or capacitance will influence the cutoff frequency and change the impedance matching, but both by only a small margin.

In conclusion, the CLC approach offers the advantages that it considerably increases the operating frequency while it only requires a very small on-chip area and only has a very small insertion loss. Also, it is quite robust against fabrication tolerances. Its disadvantage is that it is limited to roughly up to 100 GHz due to its low-pass behavior.

C. LCL Low-Pass

A very similar approach uses a 50 Ω on-chip pad and adds a fully off-chip compensation network using a parallel capacitance as well as a series inductance [5], [10]–[16], thereby forming a T-section low-pass filter. The resulting structure as well as its schematic representation is shown in Fig. 5.

The cutoff frequency of this low-pass filter is also given by (4) but only amounts to half of the cutoff frequency of the CLC filter. This is because here the filter inductance is twice the bond-wire inductance, whereas the filter inductance is equal to the bond-wire inductance for the CLC approach. This drawback can be mitigated to some extent by using double or V bonds.

In comparison to the CLC approach, the LCL approach offers the advantage that its compensation structure only consumes off-chip area. Its disadvantage is its relatively low cutoff frequency.

D. Multi-Stage LC Low-Pass

The operating frequency range of the simple low-pass approaches can be further increased by increasing the stage count of the filter to form a multistage LC low-pass [17]–[25]. Here, stage count refers to the number of passive elements used in the filter, e.g. the CLC low-pass is considered a three-stage filter. From basic filter theory it follows that the center inductance (in this case, the bond-wire inductance) increases with increasing stage count while the cutoff frequency of the filter stays constant, or that for a higher stage count the cutoff frequency increases if the center inductance (or bond-wire) stays constant, respectively. Referring also to [18], stage counts up to seven are feasible, as at even higher stage count both insertion loss and area consumption become unreasonably large.

For example, the five-stage approach in [18] achieves an insertion loss below 0.3 dB at 76 GHz, whereas the seven-stage approach in [17] can only achieve an insertion loss slightly below 1 dB at the same frequency. Thus, there appears to be a tradeoff between insertion loss and bandwidth.

The layout of a seven-stage interconnect [17] is shown in Fig. 6(a). It uses a coplanar bond-wire configuration with a length of 0.175 mm. The additional inductances and capacitances are realized by short line segments. As can be observed, this approach requires a significant amount of expensive on-chip area. However, its operating frequency range extends up to 180 GHz (see Fig. 6(b)).

Like the LCL and CLC approach, this technique is quite robust against fabrication tolerances. Small deviations of the inductances and capacitances will introduce ripples in the filter response and slightly change the cutoff frequency and

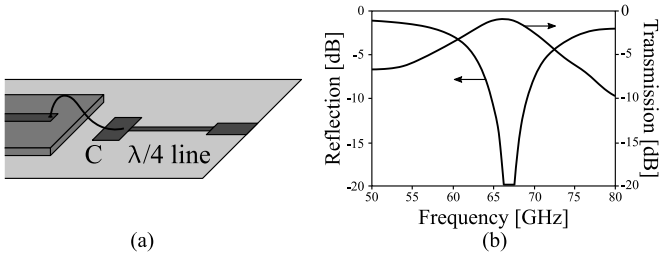

Fig. 7. (a) Layout of the $\lambda/4$ approach. (b) Simulated S-parameters. (Both from [26])

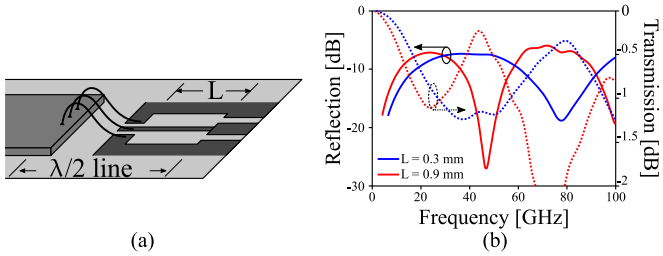

Fig. 8. (a) Layout of the $\lambda/2$ approach with additional PCB line section (embedded in epoxy, not shown). (b) Simulated S-parameters. (Both from [31])

matching, but not severely affect the functionality of the structure.

As a short summary, the advantage of this approach is that it offers a very wide bandwidth up to high millimeter-wave frequencies. Also, it is quite robust against fabrication tolerances. Its disadvantage is that it requires a large on-chip area, which is typically unwanted due to the high cost of on-chip area. However, a recent publication [20] shows that using a totally off-chip multi-stage filter is possible at the cost of sligthly reduced bandwidth. Also, increasing the stage count leads to a rather high insertion loss.

E. λ/4 Transformer

Another approach uses an off-chip $\lambda/4$ transformer [11], [26], [27]. It relies on using the smallest possible on-chip bond-pad, thereby minimizing the on-chip area consumption. Together with the bond-wire inductance and a correctly dimensioned PCB bond-pad capacitance, a real input impedance is seen from the PCB. Compared to the CLC low-pass, the on-chip capacitance is reduced and the off-chip capacitance increased. Thus, a real input impedance can be reached that is typically different from the reference impedance. Then, matching is achieved with a $\lambda/4$-long PCB transmission line section, using the well-known impedance relation:

$$Z_{\text{comp}} = \frac{Z_{\text{line}}^2}{Z_{\text{uncomp}}} \tag{5}$$

where Z_{comp} is the compensated input impedance seen from the PCB, Z_{line} is the impedance of the $\lambda/4$ line, and Z_{uncomp} is the input impedance without the $\lambda/4$ line.

Note that this relation is only valid for a very narrow frequency range, thus creating a band-pass interconnect rather than a low-pass as seen before.

The layout of such a structure is shown in Fig. 7(a), its simulated S-parameters in Fig 7(b). It can be observed that the interconnect is narrowband, but offers a very good matching in a small frequency range. Still, the insertion loss is rather high (1 dB at 67 GHz) for the design presented in [26]. This is due to the usage of two $\lambda/4$ transformers in series, which in this case was necessary because of technological constraints.

To increase the bandwidth of this approach, multiple $\lambda/4$ sections or a (Klopfenstein) taper structure can be used [20], [28]–[30]. Still, the narrow bandwidth does not only originate from the $\lambda/4$ impedance transformation, but also from the impedance transformation caused by the bond-wire inductance and the off-chip pad capacitance, which then becomes the limiting factor [20]. Also, using tapers or multiple sections may increase the insertion loss.

Due to its limited bandwidth, its dependence on exact geometrical lengths, and the condition that the imaginary parts of the bond-wire inductance and the parallel capacitance should cancel each other, this approach is quite susceptible to fabrication tolerances. Changes in bond-wire length (and thus, in inductance) will shift the frequency of the pass band and degrade the performance at the frequency of interest.

In conclusion, the $\lambda/4$ approach offers the advantages of a minimal on-chip area as well as excellent performance for a certain narrow frequency range. Still, its disadvantage is its narrow bandwidth, which may be mitigated to some extent by using multiple sections or taper structures. Also, in cases where two $\lambda/4$ transformers in series are required due to technological constraints, the insertion loss can become rather high. Due to its limited bandwidth, this approach is quite susceptible to fabrication tolerances.

F. λ/2 Line

It is well-known that a $\lambda/2$ long transmission line section transforms any impedance into itself, regardless of the line's impedance. Thus, at frequencies where the length of the bond-wire connection equals integer multiples of the half wavelength, the connection will offer near-ideal transmission (apart from insertion loss generated by the line attenuation). Notably, in this case the connection would require no compensation whatsoever, thereby also minimizing the on-chip area.

Typically, this effect occurs at a very high frequency (e.g. 0.2 mm equals $\lambda/2$ at 750 GHz). To reduce this frequency into the millimeter-wave regime, the electrical length of the bond-wire connection needs to be increased. This can be done by increasing the bond-wire length, by embedding the connection into a dielectric (e.g. epoxy), or by adding a series section of suitably dimensioned PCB transmission line [31].

A layout of this approach and the corresponding simulated S-parameters are shown in Fig. 8. In this case, a bond-wire length of 0.7 mm was used, together with a series transmission line section and embedding in an epoxy mold (ϵ_r = 3.7 and $\tan\delta$ = 0.012). It can be observed that this approach also has

TABLE I
COMPARISON OF COMPENSATION TECHNIQUES

Approach	Required on-chip area	Bandwidth	Insertion loss	Robustness against tolerances
Series Resonance	very low	very narrow (band-pass)	very low	very low
CLC	low	very wide (low-pass)	low	high
LCL	very low	wide (low-pass)	low	high
Multi-stage LC	high	ultra wide (low-pass)	low – high[a]	high
λ/4 transformer	very low	narrow[b] (band-pass)	medium	low
λ/2 line	very low	narrow[c] (band-pass)	medium	low

[a]Depends on required stage count.
[b]Can be increased by using multiple sections or a taper.
[c]Depends on bond-wire line impedance.

a band-pass behavior due to its wavelength dependency. Note that the bandwidth depends on how much the impedance of the bond-wire transmission line deviates from the reference impedance - if both were the same, an infinite bandwidth would theoretically be achieved. Also note that this approach is very sensitive to the length of the interconnect (compare Fig. 8(b)) and thus very susceptible to length tolerances of the bond-wires. Also, the impedance and thus the bandwidth of the interconnect depends on the spacing of the bond-wires, which is also prone to tolerances.

Another advantage of this approach is its low insertion loss (0.4 dB at 80 GHz [31]) even at very high frequencies.

It can be concluded that this approach offers the advantages of very low on-chip area as well as an excellent performance for a narrow frequency range. Also, the required relatively long bond-wire length leads to relaxed fabrication tolerances of the IC and PCB. The disadvantages of this approach are its rather narrow bandwidth and the high sensitivity to bond-wire length and spacing tolerances. The bandwidth, however, can be increased by matching the line impedance of the bond-wire connection as close as possible to the reference impedance, for example by adding a metal ground structure beneath the bond-wires to increase the capacitance [32].

G. Comparison of Approaches

Tab. I gives a short comparison of the bond-wire impedance compensation approaches presented so far.

The approaches that offer the lowest insertion loss due to the low number of required components are the series resonance and the CLC/LCL low-pass structures. The multi-stage LC approach can also offer low insertion loss, but as the bandwidth increases and thus a larger stage count is required, the insertion loss also increases.

Therefore, the insertion loss of the multi-stage LC approach may be lower than that of the $\lambda/4$ or $\lambda/2$ approach at some frequencies, and higher at others. More precisely, this comparison depends on the frequency of interest, as this defines the stage count of the multi-stage LC approach. Roughly, for frequencies below 100 GHz, the multi-stage LC approach will have less insertion loss, while at frequencies above 100 GHz, the $\lambda/4$ and $\lambda/2$ approaches will have less insertion loss.

IV. CONCLUSION

This paper presented several state-of-the-art approaches to compensate the effect of a bond-wire at millimeter-wave frequencies. First, the theoretical limits of an uncompensated bond-wire connection were discussed. Then, different compensation approaches were shown and compared regarding their on-chip area consumption, bandwidth, insertion loss, and robustness against fabrication tolerances. While it is not possible to give general recommendations, such as which approach to use for which frequency range, the information presented in this paper can be helpful to select an appropriate solution to a specific bond-wire interconnect problem. With the given variety of compensation approaches, wire bonding can be considered a viable solution even at millimeter-wave frequencies.

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Temperature Measurement Methods in GaN Power Semiconductors

Gayathri Latha Velayutham
dept. Electrical Engineering
University of Stuttgart
Stuttgart, Germany
st168322@stud.uni-stuttgart.de

***Abstract*—The on-line junction temperature of the device under operating condition has a significant effect on the performance, robustness and reliability of the system.Therefore, the ability to monitor the real-time junction temperature is a key in the design of reliable power system. There are numerous methods for measuring the temperature of an operating semiconductor device.The paper presents theoretical analyses of the temperature measurement in Gallium Nitride(GaN) power semiconductor. The methods can be broadly placed into three categories: electrical, optical, and physical contacts. The fundamentals underlying each of the categories are discussed, and a review of the variety of techniques within each category is given. Some of the advantages and disadvantages are also provided. In addition, it can be also used as a damage indicator and prolong the lifetime of the system.**

***Index Terms*—Gallium nitride(GaN), temperature sensor, thermal analysis**

I. Introduction

Gallium nitride (GaN) material has superior physical properties such as large band gap(3,4eV), break down fields, high saturation electron drift velocity and high thermal conductivity, which provide GaN based semiconductor devices great potential for application in high temperature, high power and microwaves fields. Temperature has significant influence on both performance and reliability of semiconductor devices. The increasing temperature will reduces crucial device parameters such as the electron saturation velocity, carrier mobility, output power, and the gain. It is also commonly assumed that the reliability of a semiconductor device decreases as the temperature increases. The act of measuring the temperature is in reality the measurement of some physical phenomena which itself is affected or changed by temperature. The physical phenomena by which the temperature of a device makes itself known are many and varied, and thus a wide range of methods have been employed for measuring and predicting the temperature at which devices operate. Both direct and indirect methods can be utilized to obtain the device junction temperature. For semiconductor devices, the useful temperature measurement methods can be divided into the broad, generic categories of electrical methods, optical methods, and physically contacting methods.

II. Basic Principles of Temperature Measurements with TSEPs

Electrical methods are routinely used to determine the active region temperature rise of semiconductor devices, which are noninvasive, fast, and can be performed using widely available, standard equipment. Electrical method uses device parameter such as forward channel resistance, threshold voltage, and the source-drain saturation current as temperature sensitive parameter (TSP).Temperature sensor and current sensor on the chip is the most effective eay of measuring temperature of the system. However, for a power devices like GaN HEMT temperature sensitive electrical parameters(TSEPs) can be an alternative method. It is an indirect way to measure temperature which is based on the temperature dependency of electrical parameters. GaN HEMT devices are investigated and compared with six different TSEPs namely source-drain reverse bias voltage (VSD), static on-resistance (RDS,ON), gate threshold voltage (VGS(TH)), transconductance (gm) switching transients (dIDS/dt) and gate current (IG).

III. Methodolgy

The caliberation is the important procedure where the relationship between TSEPs and the temperature of the device is determined using the external source. By using the hot plate, the experiment temperature is set from 25oC to 150oC with the step of 25oC and the values of electrical parameter can be noted as the temperature changes. The temperature characteristics for six different TSEPs can be seen below:

A. Source-drain reverse bias voltage

Under the test condition of VGS = 0V and IS = 1.0A, the source drain voltage increases slightly as the temperature increases and the calculated temperature sensitivity is 0.141 mV/oC. If the source-drain bias current is set ti higher value, a higher resolution can be achieved. However, the effect of self-heating would result in inaccurate result.

B. Static on-resistance

RDS,ON is measured with test conditions IGS = 10mA under 0.1A drain bias current. With temperature sensitivity 1.064 m/oC, static on resistance shows linear variation as the temperature increases.

C. Gate threshold voltage

The VGS(TH) was measured when the drain current reaches to 0.2mA. It can be observed that VGS(TH) decreases linearly with temperature and the corresponding temperature sensitivity is 1.135 mV/oC.

D. Transconductance

The transconductance can be calculated by varing VGS from 2V to 3V with 1.5V drain-source bias voltage. During this, the effect of self-heating is small and noticeable changes of IDS were observed. gm is calculated based on the equation gm = dIds/dVgs and it is inversely proportional to the temperature. The calculated temperature sensitivity is 6.330 mS/oC.

E. Switching transients

However, in the investigation of switching transients the temperature dependencies were observed for both dIDS/dt and dVGS/dt. The switching rate for both turn ON and turn OFF transients remain the same with the increasing of temperature. The only difference is the time delay on the switching of the device when the temperature increases. The estimated temperature sensitivity of turn ON delay is around 0.04 ns/oC and that of turn OFF delay is approximately 0.05 ns/oC. These temperature sensitivities are very low and it is difficult to achieve accurate temperature measurement. Therefore, based on the experiment results, the dIDS/dt is not a suitable TSEP for GaN HEMT.

F. Gate current

The temperature dependency of gate current can be calculated with 1A saturation drain-source current and 9.7V gate-source bias voltage. Here the effect of self-heating is low since the drain current is in relatively low level. In order to achieve 3.5V on the gate of the device, 9.7V gate bias voltage was selected. Gate current shows linear variation with temperature and increases with temperature. The corresponding temperature sensitivity is 2.458 mA/oC.

G. Comparison and Conclusion

Six TSEPs including source-drain reverse bias voltage (VSD), static on-resistance (RDS,ON), gate threshold voltage (VGS(TH)), transconductance (gm), dIDS/dt switching transients and gate current (IG) are investigated and then compared based on four criteria: temperature sensitivity, linearity, material and the capability of on-line temperature monitoring. The HEMT device shows no noticeable changes for VSD and dIDS/dt. The Vsd almost remains constant with increase in temperature. The temperature depedancy of switching delay are also observed when it is in both turn ON and OFF transients. This also shows very low time delays and accurate temperature measurement is not observed. While gate current shows a linear variation with sensitivity of 2.458 mA/oC. Similar results are seen in static ON resistance. The gate threshols voltage and trans conductance are inversely proportional to the temperature. In terms of temperature sensitivity. The TSEP gate current Ig can be considered for real time application for temperature measurement.

H. Advantages and Disadvantages

Advantages of electrical methods are that they are non-contacting and are the only type that can be made on fully packaged devices. The major disadvantages are the fact that the spatial resolution can not usually be well determined and that only a single, averaged temperature is measured for a device that usually has some temperature distribution

IV. Optical Methods

There are a large variety of temperature sensitive physical phenomena that can be sensed by optical methods for indicating the temperature of a semiconductor device. The most commonly used optical technique is the measurement of the naturally emitted infrared radiation from a heated body through Raman Spectroscopy and infrared camera.

A. Raman Spectroscopy

Micro-Raman spectroscopy measurements have been performed under Labram micro-Raman system with the 514.5 nm line of an Argon-ion laser as an excitation source. Measurements are performed both from top and backside. The diameter and the power of the laser spot at the device surface have been fixed at 1 m and 20mW respectively. The devices were scanned underneath the laser beam in steps of 5micrometer using a computer controller XY stage to obtain temperature maps of a half- HEMT structure. Accurate phonon frequency shift resolutions of 0.1 cm-1 have been achieved. This corresponds to a temperature accuracy of better than 10°C. Heating an HEMT using a hot-stage and measuring the temperature by Raman spectroscopy confirmed this temperature accuracy. No significant amount of laser light was absorbed(will affect self-heating) in the AlGaN/GaN HEMT during the Raman experiments due to the laser photon energy being lower than the GaN bandgap, i.e. the devices are transparent to the laser. This minimizes the influence of Raman spectroscopy on the active device during the temperature measurement. In a first step, without DC polarisation, a temperature stage with a quartz window was used to heat the sample from 300 K to 600 K. For each measurement point, the temperature was stabilized for 5 minutes before acquiring a spectrum for 1 min.

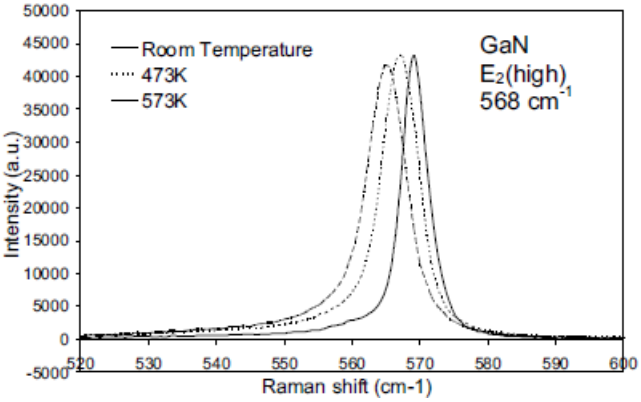

Fig. 1. Raman scattering of GaN at room temperature

In Fig 1, we show typical Raman spectra of GaN at three temperatures. in the ON-state of the devices by measuring the Raman frequency shift at different power levels. Experiments are performed at different power levels by varying the drain voltage, however, keeping its value below 20 V in order to suppress the misleading frequency shift due to the piezoelectric effect of GaN at high electric fields.

B. Infrared thermography

Infrared thermography is based on Planck's law of black body radiation. However, Planck's law was derived for a black body, a perfect absorber material that does not reflect or transmit any light. For materials that are not a perfec black body, a correction has to be made, which is called the emissivity, the ratio of the actual material radiance to that of a perfect black body as predicted by Planck's law for the same temperature and wavelength. The temperature was measured during load-pull measurements in the various conditions using a load-pull setup under the IR microscope. The wafer was placed onto a thermal chuck and infrared imaging of the surface was carried out. To calibrate the infrared microscope one has to measure the intensity of infrared radiation of the investigated part of a non-biased device heated to a known temperature (in our case 150 °C and 170 °C) measured using a thermocouple. From this measurement, emissivity can be calculated for each pixel. The resulting emissivity map is then used to compute the temperature from the raw-infrared intensity-data of the powered device. Another emissivity that had to be taken into account is the changing emissivity of the electronic circuit of the infrared microscope itself. Following this calibration, thermal scans at different dissipated power levels of AlGaN/GaN HEMT were acquired.

C. Disadvantages

Optical methods using an infrared camera and physically contacting methods, i.e., adding contact temperature detectors to the power devices, are widely used to obtain the temperature. However, due to the slow response, these methods are ill-suited for applications that require high bandwidth.

SCHOTTKY CONTACT DEGRADATION

The temperature dependence of the Schottky voltage under a forward constant current was used as a means to measure the transient temperature characteristics of gallium nitride (GaN) high-electron-mobility transistors (HEMTs). The forward Schottky voltage behavior at constant currents of 0.2, 0.35, 0.5, 1, 1.5, and 2 mA was monitored. In particular, the vertical temperature distribution was corrected experimentally based on the transient voltage measurements. The temperature dependences of the pulsed gate–diode resistance and threshold voltage extracted from the Schottky gate–diode forward characteristics of HEMTs have been proposed as the temperature sensitive parameters to measure their channel temperature. In addition, the Schottky junction voltage under a small forward current was used as a means to determine the channel temperature. Therefore, the temperature dependence of Schottky diode characteristics is potentially useful for characterizing the self heating effect in GaN HEMTs. This method increases the accuracy of temperature measurements when the temperature dependence of the Schottky voltage is used to characterize the behavior of GaN HEMTs. However, the degradation of Schottky contacts under positive gate bias makes it difficult to accurately measure their transient temperature behavior and thus leads to error in the evaluation of the temperature distribution of the vertical multilayer structure. Therefore, it is necessary to remove the effect of Schottky degradation from transient temperature measurements.

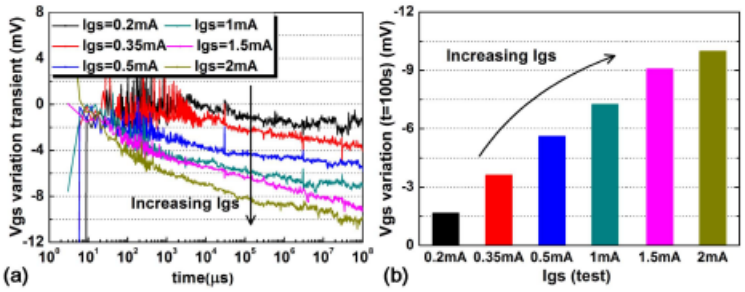

Fig. 2. (a) Variation of the Schottky voltage at forward Schottky test currents Igs of 0.2, 0.35, 0.5, 1, 1.5, and 2 mA over the time period from 1 s to 100 s. (b) Dependence of the Schottky voltage variation at a time of 100 s on Igs.

CONCLUSION

There are a wide variety of methods exist for measuring the temperature of GaN power semiconductor device. Methods that use electrical parameters of the device as the thermometer have the advantage that the temperature of fully packaged devices can be measured, but they do not allow two dimensional temperature maps to be made. Another advantage of electrical techniques is that they only require the use of standard electronic instrumentation for the measurement. Optical method shows a slow response, which is not suitable for applications that require high bandwidth. The fact that the surface of the device being measured must be available for contacting (thus packaged chips can not be measured) and the thermal response depends upon the response of the probe, which may be considerably slower than that of the device. By comparing the advantages and disadvantages of all the methods, electrical parameters seems to be more reliable.

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Dynamic loss mechanism of wide bandgap semiconductor (GaN) HEMTs due to On-State Resistance

Choudhury Asbha Alam
University of Stuttgart
Stuttgart, Germany
st168927@stud.uni-stuttgart.de

***Abstract*—Gallium Nitride (GaN) transistors are popular for use in power electronics because of their low resistance and capacitance as compared to Silicon devices, but after switching operation GaN transistors expose higher on resistance than the resistance quoted in the data sheet due to trapping effect which increases device On-Resistance R_{DSON} values. In this paper, we present some comparison among several researches for the extraction of dynamic On-Resistance and evaluate the most convenient and precise technique to extract R_{DSON} as well as behaviour of R_{DSON} for two different GaN transistors. Furthermore, the dynamic R_{DSON} behaviour of these two types of GaN transistors are tested under hard switching and soft switching conditions by double-pulse and multi-pulse test modes respectively.**

***Index Terms*—Gallium Nitride (GaN), On Resistance, Double pulse test, Multi pulse test, Current collapse, Hard switching, Soft switching**

I. Introduction

Application of GaN (wide bandgap semiconductor) device is becoming more and more popular in power electronics systems design, because GaN device can operate at high temperature, switch faster and produce low power loss [1], and the dynamic loss power of a GaN transistor depends on it's R_{DSON} which also changes with different parameters. For better usage of GaN devices, it's really important to understand their characteristics. Because of small device ON-state resistance and inter-electrode capacitance GaN device has better performance in electrical energy conversion [1]. However, due to the trapping of electron in the device it exposes higher ON-state resistance when it's switched from high off state voltage and frequency and it causes dynamic on state resistance R_{DSON} which is a drawback of GaN transistors and so far the biggest challenge for GaN based transistors [2]. The trapping effect mainly occurs as surface trapping, interface trapping and buffer layer trapping which is shown in fig. 1, where the surface traps and interface traps known as shallow traps and buffer layer traps know as deep traps. All the trapped electrons are not freed instantaneously when device changes from OFF-state to ON-state, which reduces device ON-state current carrying capability by two dimensional electron gas (2DEG), trapped electrons positions and their influence on 2DEG is illustrated in Fig. 1. Some techniques are introduced to alleviate the trapping effect are discussed in [15]-[16].

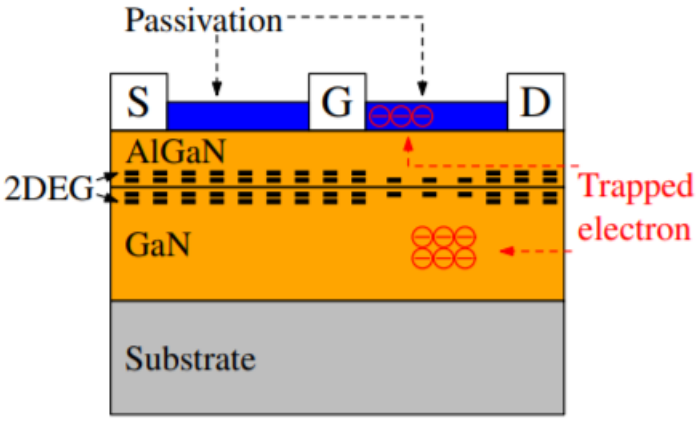


Fig.:1 Trapped electrons positions and their influence on 2DEG in GaN-HEMT [1]

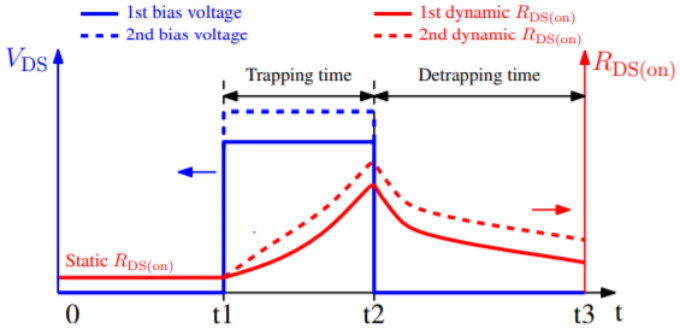


Fig.2: GaN-HEMT dynamic RDS(on) values due to trapping effect [1]

Illustrated in Fig. 2, this trapping effect is related mainly with two parameters when device in OFF-state, one is the bias V_{DS} voltage value and another is the bias time (trapping time), which would give rise to the increase of GaN device ON-state resistance R_{DSON} value. In the ON-state, detrapping process occurs and the R_{DSON} values decrease to the static value at a rate characterized by detrapping time [1]. When employing GaN transistors in power electronics circuits, GaN device might switch with different periods and duty cycles leading to a combination of trapping and detrapping effects and consequently uncertainty in the actual value of R_{DSON}, this will lead to uncertainty in device power loss, making

predictions of converter efficiency and cooling system design challenging. The ability to characterise and model GaN HEMT R_{DSON} values is thus an important design consideration [1].

The most commonly used method for characterizing device trapping and current collapse is the pulsed Current-Voltage I-V measurement which mainly focuses on device characteristics and mechanism analysis [3], most of the researches approached through this method for extracting dynamic on resistance. However, this method induces high contact resistance and is not able to capture device behaviour correctly during and immediately after fast switching transient which is described in [4]. So, we selected a circuit from the available test circuits what will be sufficient for the measurement of dynamic characteristics under different conditions (Hard Switching, Soft Switching and different voltage and frequency range).

TABLE I
SUMMARY OF DEVICES UNDER TEST

Parameters	Device A	Device B	Device C
Voltage/Current Rating	600V/35A	650V/30A	600V/13A
Technology	CoolMOS™	E-mode (p-gate)	E-mode (X-GaN GIT)
Package	TO-220	GaNPX®	DFN 8×8
R_{DSON}*	53(52/60) mΩ	46(50/63) mΩ	150(140/190) mΩ

*The R_{DSON} values are extracted from the output curves measured by curve tracer at room temperature and the R_{DSON} typical/maximum values from datasheet at 25 °C are also given in parenthesis for reference.[4]

(Double pulse test) DPT is widely used method to investigate different parameters of a DUT (device under test) as well as for the extraction of dynamic R_{DSON} where the DUT only switches under Hard Switching Condition [5]-[8]. In [10], the dynamic R_{DSON} characteristics under the two switching conditions are evaluated by independently controlling the gate and drain pulses, where the measurement method and circuit are not yet properly interpreted. The zero voltage turn-on circuits are good choice for GaN based converter at high frequency application because, GaN device's turn-on switching loss is much more higher than turn-off switching loss [4], however, this is also true for hard switching. Therefore, from application prospective, the current DPTs or other Hard Switching circuits are not sufficient for broader investigation of Dynamic On Resistance. In the available researches few test circuits operating in soft switching mode have been built for R_{DSON} evaluation. A zero voltage transition (ZVT) circuit was employed in [2] for GaN device evaluation for both hard and soft switching conditions. Although the ZVT branch can be easily connected and disconnected to the conventional DPT, the additional resonant inductor and auxiliary complicate the test circuit, a resonance-based soft switching circuit is proposed in [17]. Although there is no voltage or current spikes in the measured waveforms, a long delay time of R_{DSON} measurement still exists and the duty ratio is limited in order to realize zero-voltage-switching (ZVS) conditions which are discussed in [4].

In this paper, we discuss about a circuit which is useful and can be easily implemented from the conventional DPT (Double Pulse Test) and compare the result and mechanism with other test setups. In addition, this method can be useful for comprehensive investigation of Dynamic R_{DSON} in both Hard switching and soft switching conditions [4]. This circuit is very simple and has fewer components but a widely used soft switching techniques from [11] is used to compare the on resistance under different switching conditions. This developed circuit is used to investigate the Dynamic R_{DSON} of two different GaN devices and one MOSFET in Table:1, and their behavioural comparisons are presented as well.

II. DYNAMIC ON-STATE RESISTANCE MEASUREMENT OF GAN-HEMT

A. Measurement circuit

Dynamic on-state resistance R_{DSON} of GaN device can be measured by device on-state voltage V_{DS} across it and drain current I_D through it in a test set-up. As the measured bias voltage when the device is off-state could achieve more than multiple several times higher than device $V_{DS(on)}$ therefore, a voltage clamping circuit is necessary. So a bias circuit is constructed.

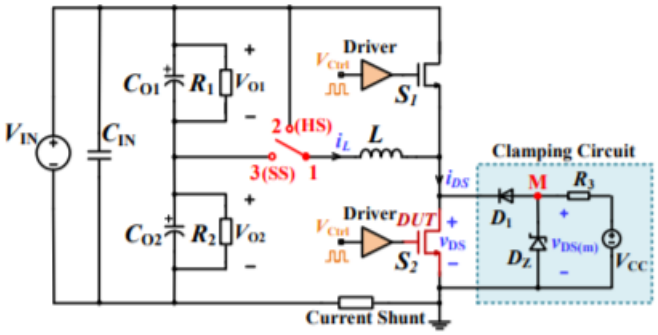


Fig.3:Test circuit in half-bridge configuration with clamping circuit. The circuit can realize hard switching (HS) test by connecting 1 to 2 and soft switching(SS) test by connecting 1 to 3. [4]

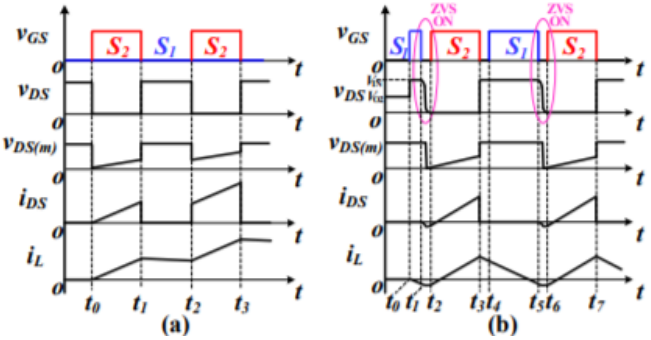


Fig.4: Control signals and related voltage/current waveforms under (a) hard switching condition and (b) soft switching condition. [4]

In this paper, two test circuits are discussed to observe the variation of R_{DSON}, one is commonly used DPT with

half bridge configuration for hard Switching condition and another one is the TCM (triangular current mode) test circuit for soft switching condition. The two circuits are integrated into one test board to ensure that a GaN device can be tested by different circuits in the same test setup [4]. As shown in Fig. 3 the test circuit can be built for Hard switching condition if terminal 1 to 2 is connected, the related control signals with voltage/current waveforms are given in Fig. 4 (a). Here, the inductor current freewheeling path is provided by the upper device operating in reverse conduction mode [4]. On the other hand, if terminal 1 to 3 is connected, this test circuit acts as a TCM test circuit for soft switching condition. It is similar to a synchronous Buck converter, but the output capacitors have already been charged with initial values VO1 and VO2 before gate signals arrived, due to the series connection of CO1 and CO2, and therefore, it can be forced to operate in pulse-mode but steady state without initial pre-charge process for the output capacitors[4]. In Fig.4(b) we can see the control signal and related current/voltage waveforms. During the first time interval t0-t1, a short gate pulse (around 100ns) is provided to S1 and while S1 conducts, the load inductor is charged by VIN-V02 and the inductor current iL increases to a small value. During deadtime t1-t2, the parasitic capacitance of S2 discharges through L and therefore V_{DS} starts to drop, and when VDS drops to zero the channel of S2 starts to conduct reversely. As a result, S2 turns on under Zero Voltage Switching (ZVS) at t2. As S2 is turned on, the load inductor is reversely charged by VIN-VO1. The load current iL changes the direction and keeps increasing until S2 is turned off at t3[4]. At t4 S1 will turn on again after a deadtime with decreasing iL and finally turned off at t5 which leads to the next ZVS so, S2 will turn on again at t6. The deadtime used in this design is 100ns which is within a reasonable range to realise ZVS and the size of the capacitors C01 and C02 are large enough to keep V01 and V02 constant during microsecond-level test [4]. The value of V01 and V02 can be determined by resistors R1 and R2, which enables the converter to go directly into steady state at different duty cycles in multi-pulse test mode and here, R1, R2 are the same to match 50% of duty cycle [4]. As it has been mentioned about the clamping circuit,it plays the key role for the measurement mechanism, the voltage across the Zener diode $V_{DS(m)}$ is measured instead of the voltage V_{DS} cross DUT. During the off-state of DUT, the diode D1 is off, so $V_{DS(m)}$ is clamped to the Zener voltage of DZ, which is much lower than V_{DS}. When DUT is turned on, the junction capacitance of D1 is discharged until D1 is turned on. As a result,$V_{DS(m)}$ represents the sum of V_{DS} and the diode forward voltage VD1 [4]. Different from that in [5], VD1 here is calibrated rather than using a constant value in that the variation of VD1 will affect measurement accuracy especially for low R_{DSON} and the characteristics of D1 and the needed fitting formula described in [4] for the calibration of VD1. The value of R3 is chosen in such a way so that the forward current IF keeps low in order to avoid the increasing junction temperature.s. The I-V characteristics of D1 shown in [4] are measured by Agilent HP4155B semiconductor parameter analyzer. The junction capacitance of D1 caused the some ringing effect therefore, the valid R_{DSON} data should be taken with 150ns delay after the turn on transient, although a SiC Schottky diode (CSD01060) with small parasitic capacitance is used here[4]. Four-layer PCB is produced in such a way that it won't influence the test result with it's influential characteristics for instance low parasitic inductance. In [4] three test boards were produced with same configuration to accommodate different packages of the tree types of devices. In more detail, an isolated half-bridge driver IC ADUM3223 is used with 10 Ω turn-on gate resistor and 5 Ω turn-off gate resistor respectively [4]. The drain current is measured with a 0.1 Ω coaxial shunt (SSDN-10) from TM Research Inc. A SMA connector with coaxial cable is used to sense the clamping voltage. For more accurate measurement of RDS(on), it is necessary to ensure that the propagation delay between voltage and current probes are calibrated before measurement. The alignment of voltage and current measurement is achieved by replacing the DUT with a low inductance resistor and measuring the voltage and current of the resistor at the same time [12].

Fig.5: Photo of the experimental setup for measuring dynamic on-state resistance

On the other hand, in [9] it is presented a method for the extraction dynamic on-state resistance under hard and soft switching conditions and they implemented different test setups which are complex compare to the test setup that is discussed in this paper, however, a voltage clamping circuit is constructed with that setup which is similar to this circuit that is discussed here.

III. DOUBLE-PULSE TEST UNDER HARD AND SOFT SWITCHING CONDITIONS[4]

A. Dynamic On-Resistance Measurement Method

With the following equation the dynamic on-state resistance is simply being measured in different researches where on-state voltage and current across the device is captured. R_{DSON}=V_{DSON}/I_{DSON} However, for this circuit which we discussed, the dynamic on resistance is measured with the following equation R_{DSON}=(V_{DSON}-V_{D1})/I_{DS}.

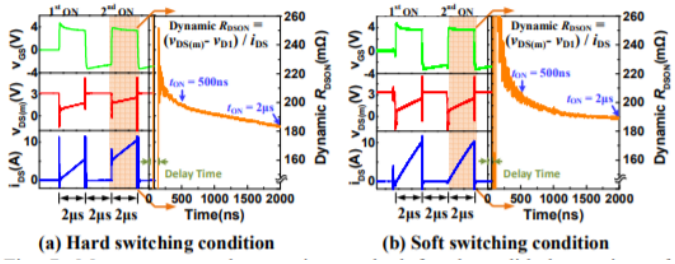


Fig.6: Measurement and extraction method for valid data points of dynamic R_{DSON} in Double pulse operating mode. The time slot for the R_{DSON} measuring is shown in shadow region[4]

In this section the measurement and extraction method of dynamic on resistance is discussed and also compared with other researches for both hard and soft switching conditions. In fig. 6 the methods are described in Double-pulse operating mode. Here the pulse duration 2μs, so, DUT conducts 2μs during the first pulse. after a short interval of 2μs the DUT turns on again and this second on state time is highlighted in Fig. 6 in which the variation of R_{DSON} is measured and calculated. Since R_{DSON} is not a constant value and gradually decreases after switching from high off-state voltage,the R_{DSON} at 500 ns (the beginning of conduction) and 2μs (the end of conduction) are extracted and described in this process [4]. In order to avoid the switching noise at the beginning of conduction, 500 ns is selected. Here, the Dynamic R_{DSON} is measured under different voltage stress from 100V to 400V where 50V per step with same drain current. The same drain current under different voltage stresses can be maintained by adjusting the value of the external inductor proportionally [4].

In contrast, other methods that implemented Double pulse test for extracting dynamic on-state resistance presented similar characteristics of dynamic behaviour of GaN devices under both hard switching and soft switching conditions. For instance according to [2], in contrast to the soft switching circuit, a hard-switched power transistor has additional switching losses due to the presence of high voltage and current stress during it's switching transient, which could cause additional trapping or degradation due to channel hot electrons in GaN transistors. In [2], the dynamic R_{DSON} was measured after 2μs after the device switched on for both hard and soft switching conditions similar to [4] and both presented similar dynamic behaviour of GaN transistors which is a decrease of on-state resistance after the device was turned on what is indicating detrapping transient.

B. Experimental Results for Double-Pulse Mode Operation

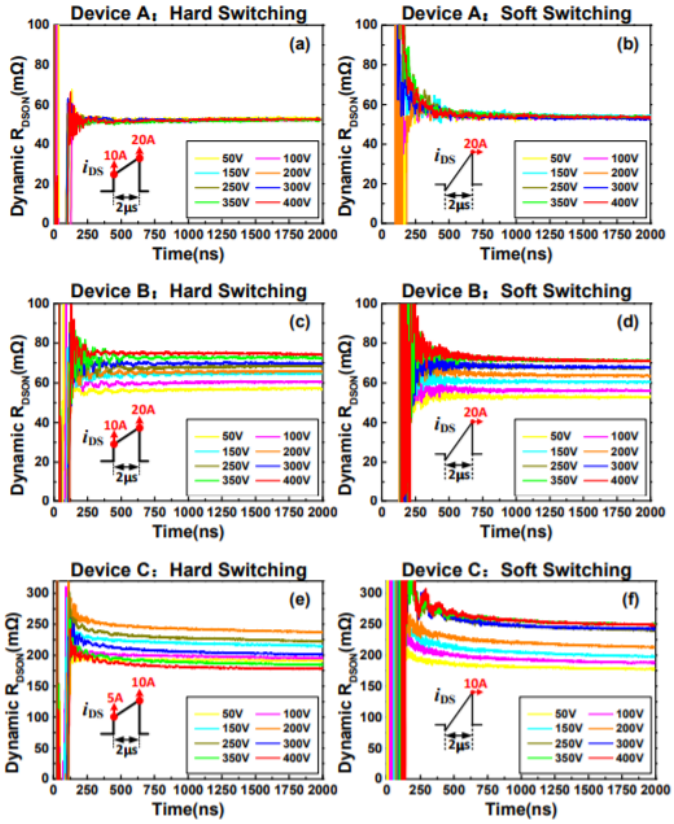


Fig.7 : Dynamic (R_{DSON}) under hard and soft switching conditions with different voltage stresses from 50 V to 400 V with the same drain current. (a), (b) Device A. (c), (d) Device B. (e), (f) Device C. Inset: Drain current variation during the measurement period.[4]

Fig. 6 represents the variations of R_{DSON} which is measured for for three different devices (device A,B,C) under hard and soft switching conditions.The origin of the time axis is selected when the VGS of DUT begins to rise. The delay time is observed within 150 ns, and in this initial part R_{DSON} data is missing and it should be noted that under Soft Switching condition the large oscillation during 500 ns are caused by low iDS at the beginning of conduction.

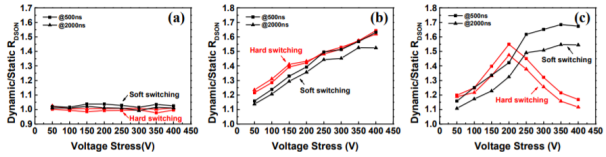


Fig. 8. Dynamic/Static R_{DSON} values at 500 ns and 2000 ns after turn on from different voltage stresses under hard and soft switching conditions. (a) Device A. (b) Device B. (c)

Device C.[4]

The measured R_{DSON} values are normalized by the static R_{DSON} extracted from output curves measured by curve tracer at room temperature. The dynamic/static R_{DSON} values at 500 ns and 2000 ns after turn on from different voltage stresses under hard and soft switching conditions are plotted in Fig. 8 [4]. In this comparison, it's clear that three devices show different variation of dynamic resistance under different voltage stress. It was predicted that device A has no noticeable effect in both switching conditions as it's a CoolMOS device but device B and C show different behaviour. Device B shows (in Fig. 8) similar variation trend in both switching condition with increasing voltage stresses but device C shows non-monotonic behaviour under hard switching with voltage stresses. The maximum R_{DSON} can be deduced at the turning voltage stress which is between 200 V and 250 V. It is observed that the dynamic R_{DSON} in the DUT is nearly the same to the static R_{DSON} under high voltage stress (400 V). Secondly, an obvious increase of dynamic R_{DSON} under soft switching condition is observed, which is more severe under high voltage switching condition (400 V). Similar phenomenon has been shown in [16] where the GaN HFETs under test showed higher R_{DSON} under soft switching condition, but the physical mechanism is different due to the different device structures between device C here and the DUT in [10]. Finally, as compare to hard switching condition the soft switching condition results in lower R_{DSON} below the turning voltage stress but higher R_{DSON} above the turning voltage. The variation of the experimental results occurred because of different device technologies of device B and device C. For device C, it's fabricated with an additional p-GaN structure in the vicinity of the drain electrode PD, which doesn't exist in device B. The attribute of R_{DSON} due to PD and the inside mechanisms will be discussed in V.

The results disclose the impact of switching conditions while measuring Dynamic on Resistance due to different device technologies so for commercial GaN devicees it's really important to consider the switching conditions in order to achieve the accurate evaluation. In comparison with [2] GaN devices and Si(Si device shows dynamic on resistance as well but it can be controlled) devices showed similar dynamic behaviour under hard and soft switching conditions which is presented in the following Figures 9(a) and 9(b). As a result, in DPT operation under both hard and soft switching conditions GaN devices show similar dynamic behavior in the available literature and that is the variation of Dynamic on-state resistance dependent on voltage stress and with associated time constant of the traps.

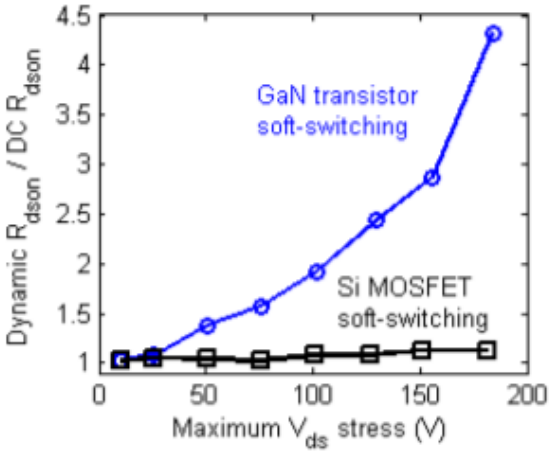


Fig:9(a) Normalized dynamic on resistance GaN transistors and Si MOSFET in soft switching condition at 2μs for different voltage stress.

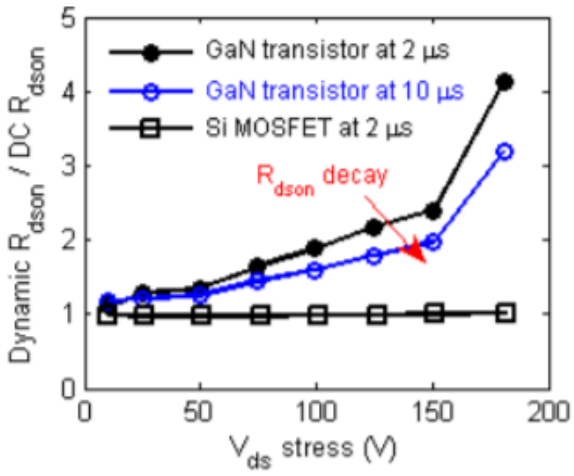


Fig:9(b) Normalized Dynamic on resistance for hard switched GaN transistor and Si MOSFET at 2μs and 10μs after the device were switched on.

IV. MULTI-PULSE TEST UNDER HARD AND SOFT SWITCHING CONDITIONS [4]

The multi-pulse test mode needs to be considered because the trapping and de-trapping effect of GaN device is similar to charging and discharging process of RC units in series with specific time constants and it suggests that the dynamic (R_{DSON}) requires sufficient time to reach steady state and the settling time could depend on switching frequency.

A. Dynamic On Resistance Measurement Method

In multi-pulse mode, device B and device C are tested. Fig. 9 illustrates the main waveforms of (R_{DSON}) evaluation in multi-pulse test mode. In order to avoid self heating, total test time is limited to 100μs. For hard switching test, the inductance load in Fig. 4(a) are replaced by RL load (resistor and inductor in series) to set up inductor volt-second balance and consequently avoid the continuous increase of drain current and for soft switching test, the test circuit is the same to that of the double-pulse test mode [4].

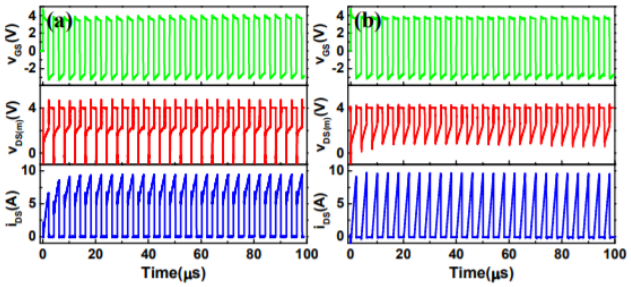


Fig. 10.Multi-pulse test waveforms at VDS=100V and f=250kHz (a)Under Hard Switching Condition (b) Under Soft Switching Condition

Here for device B and device C, (R_{DSON}) is measured under different frequency and voltage stresses (i.e. 250kHz,500kHz,1MHz and 100V to 400V) with same drain current. For, soft switching operation, during each cycle the drain current increases from zero to the steady state value. And for Hard Switching condition, the values of RL load are adjusted carefully to make sure the drain current stays the same under different conditions and drain current can reach steady state within 10μs. At the same time the impact of frequency on (R_{DSON}) is observed and the duty cycle is set as 50% in all cases[4].

B. Experiment Result for Multi-Pulse Mode Operation

In Fig.10 the dynamic R_{DSON} during total 100μs are shown and from Fig. 11(e)-(h) represents the final conduction period extensively. For device C In Fig.11 the dynamic R_{DSON} during total 100μs are shown and from Fig. 12(e)-(h) represents the final conduction period extensively. In order to reveal the R_{DSON} in quasi-steady state, the median value of dynamic on resistance is extracted for comparison and 100V and 400V conditions are shown here.

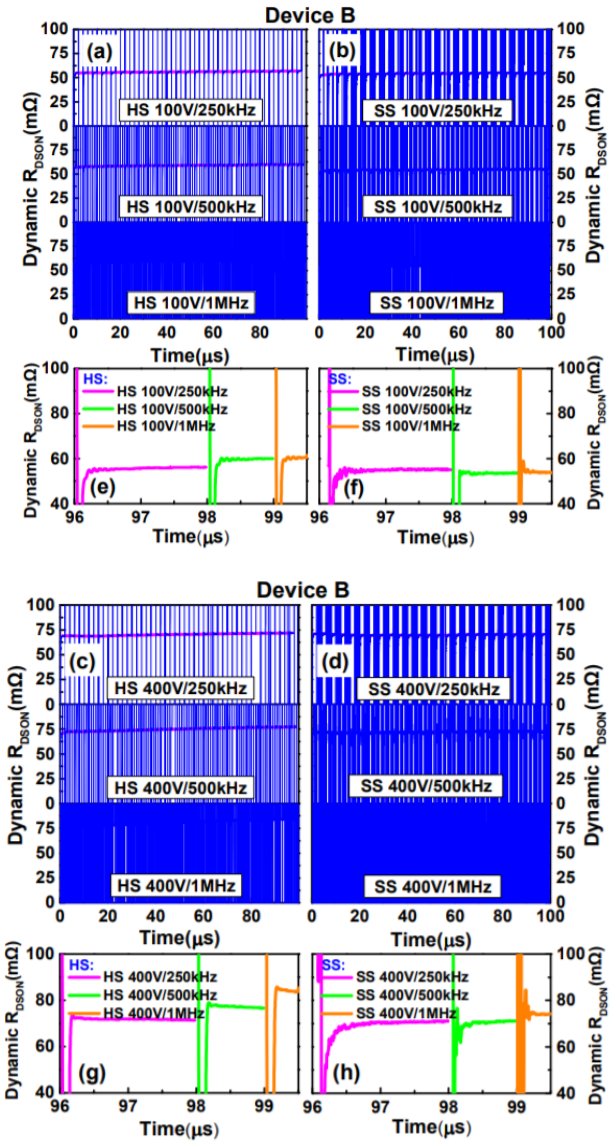
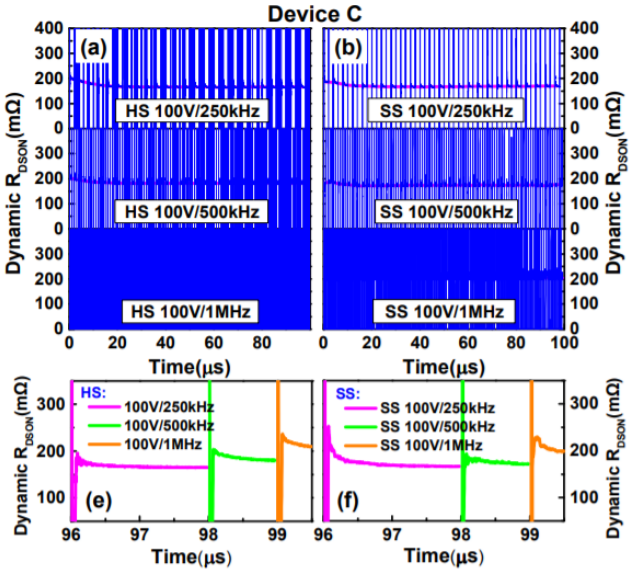


Fig. 11: Dynamic R_{DSON} variation of device B during the total 100 µs test period under hard switching (HS) and soft switching (SS) conditions with different frequencies. (a), (b) at 100 V voltage stress; (c), (d) at 400 V voltage stress; (e), (f) R_{DSON} variation during the final pulse at 100 V voltage stress with different frequencies; (g), (h) R_{DSON} variation during the final pulse at 400 V voltage stress with different frequencies.[4]

In the next figure, Fig. 12 explains the normalized R_{DSON} and how it varies with the voltage stress. Just like the previous operation(DPT), here for device B, the dynamic on resistance increases with voltage tress under both switching conditions but lower on resistance is observed under soft witching condition. For device C, it's observed non-monotonic behaviour under hard switching conditions with increasing voltage stress where there is still a turning voltage between 200V and 300V.As compared to hard switching condition, soft switching condition results lower R_{DSON} below the turning voltage but

higher R_{DSON} above turning voltage. The measured R_{DSON} are replotted in Fig. 13 with different frequency. It is well acknowledged that higher frequency results in an increase of dynamic R_{DSON} and the increase is more apparent with higher voltage stress due to more severe trapping effect [7], which coincides with the experimental results. The experimental results show that the impact of frequency on on-state resistance varies with switching conditions and device technology. As is shown in Fig. 13, for device B without PD structure, the measured R_{DSON} is relatively insensitive to the switching frequency, especially in soft switching condition and for device C with PD structure, the dynamic R_{DSON} increases with frequency under both hard and soft switching conditions. The difference in R_{DSON} under the two switching conditions is more obvious at high voltage and high frequency [4]. Particularly, while operating under 400V and 1MHz soft switching condition, the dynamic on resistance becomes close to twice to the static value which leads to a very serious current collapse.

In Fig. 12(a)-(d) the value of dynamic on resistance varies gradually to a nearly steady value with the increase of pulse number. The pulse numbers needed to reach the steady state are different with frequency and voltage stress [4]. For more clarity, the median value of R_{DSON} during each conduction period at 250kHz extracted and plotted in Fig. 14, where the results of double pulse test mode also denoted and it's obvious that for device B, DPT results are consistent well with that of multi pulse, but for device C, the DPT results can not reflect the true R_{DSON} in a steady state due to the time dependent trapping and de-trapping effect [4]. It's observed that the conventional test method using only one or two pulse may not enough with respect to dynamic R_{DSON} evaluation of current commercial GaN devices due to their different device technologies.



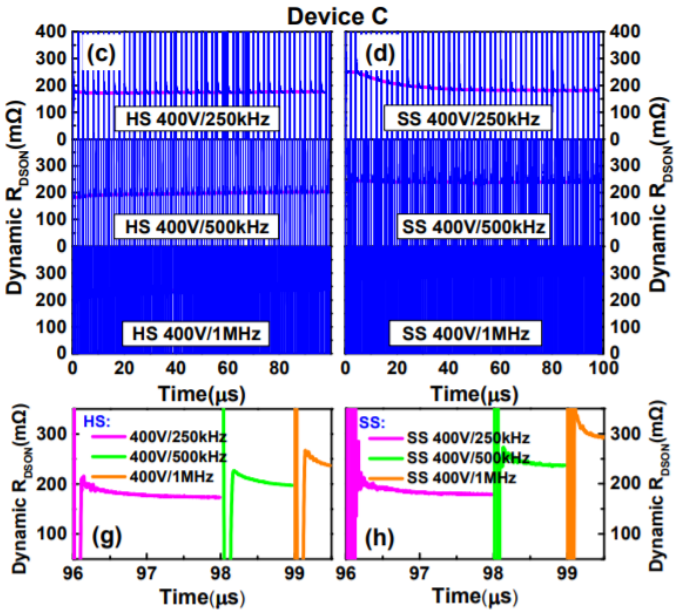


Fig. 12: Dynamic R_{DSON} variation of device C during the total 100 μs test period under hard switching (HS) and soft switching (SS) conditions with different frequencies. (a), (b) at 100 V voltage stress; (c), (d) at 400 V voltage stress; (e), (f) R_{DSON} variation during the final pulse at 100 V voltage stress with different frequencies; (g), (h) R_{DSON} variation during the final pulse at 400 V voltage stress with different frequencies.[4]

V. MECHANISM ANALYSIS[4]

Earlier researches suggest that it is more important to focus on impact of different operation parameters on dynamic on state resistance R_{DSON} such as voltage, temperature, off-state time etc. However, few of them suggested some explanation of experimental results. This section aims to further enhance the understanding of the dynamic R_{DSON} under different switching conditions and the analysis results can provide valuable information for both applications and device manufacturing[4].

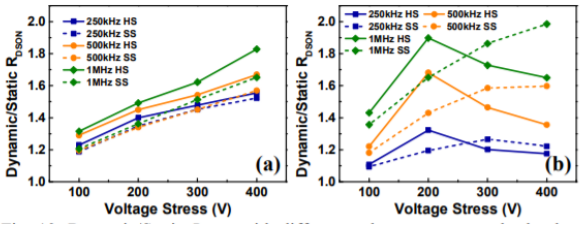


Fig.13: Dynamic/Static R_{DSON} with different voltage stresses under hard and soft switching conditions. (a) Device B. (b) Device C. [4]

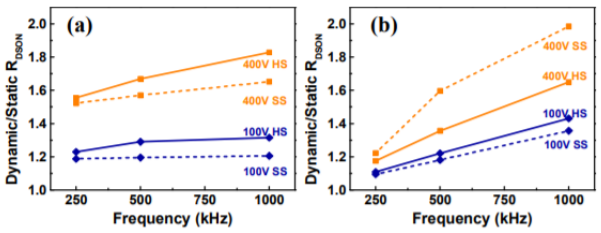


Fig. 14: Dynamic/Static (R_{DSON}) with different frequencies at 100 V and 400 V under hard and soft switching conditions. (a) Device B. (b) Device C. [4]

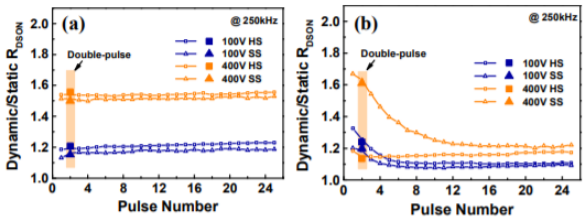


Fig.15: Dynamic/Static RDS(on) variation with pulse number at f = 250 kHz multi-pulse operating mode (symbol line). The results of double-pulse test mode are denoted by larger symbols. (a) Device B. (b) Device C.[4]

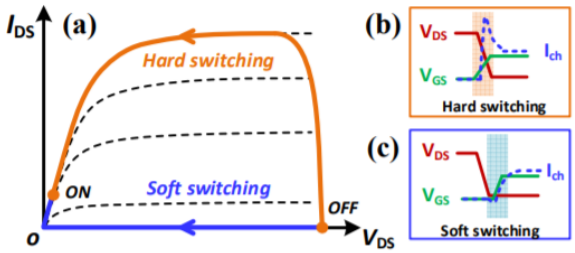


Fig 16: (a) Load line during the switching transient. (b) Hard switching transient cause high channel current. (c) Soft switching transient cause low channel current. [4]

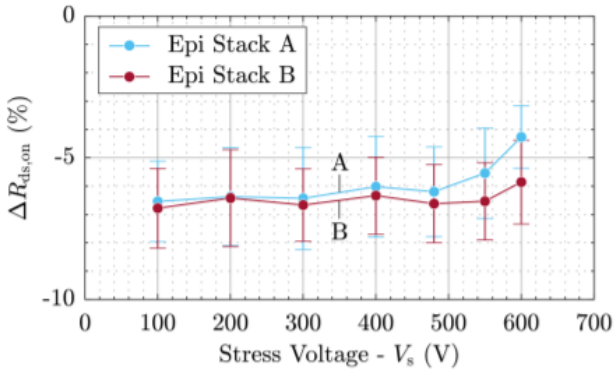


Fig.17:R_{DSON} of the two DUT featuring epitaxial stacks A and B measured in dynamic conditions as a function of voltage stressV_{DS}

The load line under different switching conditions is also presented here in Fig. 16(a), Here for hard switching the load line passes through high power area with high voltage and high current applied simultaneously that results in hot electron injection to surface traps as well as buffer trap [13]. However, for soft switching, the effect of hot electron is not prominent since the load line bypass the high-power area[4] and as a result, the (R_{DSON}) is lower under soft switching. The hot electron effect becomes more obvious at high voltage stress and high frequency under hard switching condition, which is responsible for (R_{DSON}) increase with off-state voltage and frequency [2]. The measured (R_{DSON}) is relatively insensitive to the switching frequency in soft switching condition (Fig. 14(a) due to minimal hot electron effect which usually occurs under hard switching condition[4]. Fig. 8(b) explains the behaviour R_{DSON} of device B under different switching condition where under both switching condition this device has similar R_{DSON} characteristics with off state voltage, but lower R_{DSON} in soft switching condition. The results are consistent with a general understanding of GaN devices in previous works [6,7,8] , which is attributed to enhanced hot electron effect during hard switching. Fig. 17 explained the R_{DSON} of two DUT featuring the two considered epitaxial stacks is measured under dynamic conditions and with different stress voltage Vs up to 600 V (applied across the drain and source terminals of the DUT in off-state). The results are normalized with respect to R_{DSON} measured in the same setup with Vs = 0 V (to exclude any other possible dependency, e.g. related to temperature) and compared in Fig. 17. Both DUT, i.e. epitaxial stacks A and B, exhibit a good uniformity of R_{DSON} with respect to Vs , are well comparable between each other and do not feature any increase of R_{DSON} in dynamic conditions and here epitaxial stack B is demonstrated to be equally good as A in terms of dynamic R_{DSON} in these conditions it was elaborately discussed in [18].

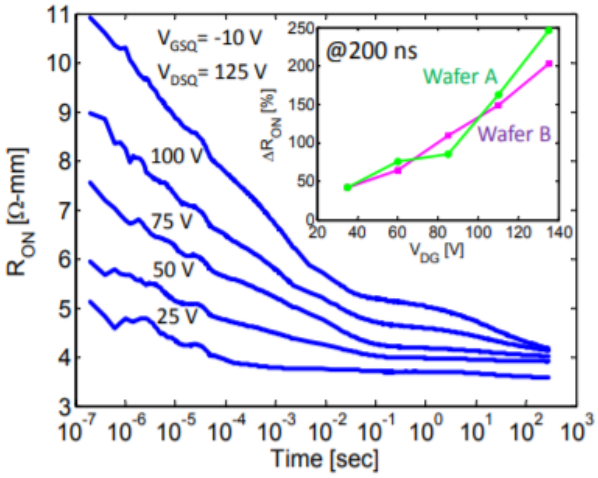


Fig.18:OFF to ON state transients from different quiescent V_{DS} conditions for different wafer

In summary, there are two distinct mechanisms that cause the non-monotonic R_{DSON} behavior of device C with increasing voltage stress under hard switching condition and When

operating below the turning voltage stress, the dominant hot electron effect results in increasing R_{DSON} with voltage stress and higher R_{DSON} under hard switching condition, as compared to soft switching condition, likewise When operating above the turning voltage stress, the hole injection effect from PD becomes more significant as the voltage stress increase, which results in decreasing R_{DSON} with voltage stress and lower R_{DSON} than soft switching condition[4]. In comparison with other approaches GaN devices have similar On-state resistance over time and highly dependent on voltage stress and after turn on transient takes some time to settle down to static behaviour which is shown in fig.18, where a significant change of On resistance is observed over time.

VI. CONCLUSION

In this paper, the variation of dynamic R_{DSON} depending on different switching conditions for different operating modes (Double pulse and multi pulse) as well as different approaches and results are discussed. In several researches, it's presented that the off-state voltage is the major contribution to the increase of dynamic R_{DSON} as charge traps increase with voltage stress, the Hard-switching transient can induce additional trapping and degeneration in GaN transistors. The variation of R_{DSON} depends on trapping and de-trapping time constants in each switching transient and in this case the Multi-pulse test that operates in a quasi-steady state is preferred to match the practical application for the evaluation of R_{DSON}.

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A Review on Substrate Integrated Waveguide (SIW) and Transition Models

Arnold Bistri
Universität Stuttgart
Stuttgart, Germany
st119861@stud.uni-stuttgart.de

***Abstract*—This paper provides a review on substrate integrated waveguides (SIW) and their transition to other transmission lines with an approach to microwave and millimeter-wave applications. SIW presents an attractive planar transmission line which shows a low loss, low cost, and can be easily integrated into microwave and millimeter-wave communications systems. A good choice of the dielectric substrate in addition to a proper design of the geometry can reduce the losses of the structure. Transitions to other transmission lines present a challenge for maintaining a broadband and low insertion loss interconnection. The most commonly used transitions from SIW and possible solutions are presented in this paper: to microstrip, coplanar waveguide, and rectangular waveguide. Moreover, a new transition from SIW directly to the chip is investigated.**

***Index Terms*—substrate integrated waveguide (SIW), transitions, microstrip, CPW, RWG, loss.**

I. Introduction

As the applications on the microwave and millimeter-wave communications are increasing, technologies such as substrate integrated waveguides are becoming widely used.

SIW present a synthesized nonplanar waveguide, which is transformed into a planar form and integrated into planar dielectric substrates by using different fabrication techniques [1]. The rectangular waveguide (RWG), employed in MMW systems has proven low insertion loss, low sensitivity and high power capability however, it remains costly and due to its bulky size and non-planar structure, makes it difficult to be integrated with the other printed circuit board (PCB) components.

Printed or etched transmission lines such as microstrip or coplanar waveguides are used for low-cost applications, which require high integration density and small size or form factor, however, these structures are subject to relatively high losses and packaging issues due to their unbounded geometry[1].

SIWs aim to overcome the limitations of classical transmission lines and present a good trade-off based on the performance, cost, size, and manufacturability compared to the other available structures. Integrating the rectangular waveguide into a substrate reduces the Q-factor due to the dielectric filling. A SIW structure manufactured with a low cost PCB technique, show much higher Q-factor compared to a low-cost microstrip line, however lower than that of a bulky high cost standard waveguide [1].

The SIW structure can be used for designing high performance passive circuits such as resonators, filters, couplers, power dividers and antennas.

By far the most convenient way of designing SIW, consist of building in a plated substrate two rows of metallic posts in parallel with a defined spacing as depicted in Fig. 1, which allows a similar propagation of EM waves as in the RWG, except the TM modes, which can not propagate in the SIW.

Except for the PCB fabrication technique other technologies have found their way into the development of the SIW. LTCC technology has also been used for developing the SIW structures and techniques such as 'ion track technology' have been used for the implementation of the SIW antennas [2]. For frequencies above 100GHz, which require a high process precision, embedded SIWs in a silicon interposer technology are proposed in [3].

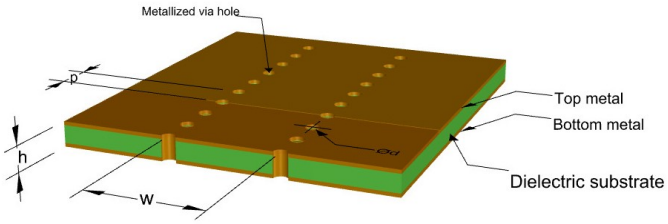

Fig. 1. Geometry of a substrate integrated waveguide.

The via trench placement, diameter and distance can cause potential wave attenuation or leakage, therefore an analytical expression has been derived in [4].

The surface current flow in the logitudinal direction is cut by the slots, which make the propagation of TM modes along the SIW impossible. If these modes would exist, they would cause a lot of radiation. For the same reason also TE_{nm} modes with m not being equal to zero have to be avoided. The dominant mode for the SIW is the TE_{10} mode, which shows an equivalent wave propagation to the conventional RWG TE_{10} mode with minimal leakage losses.

Compared to microstrip where the major losses are related to radiation, the SIWs which are self-packed, show insignificant radiation loss however, if generated, the radiation or leakage loss can lead to signal losses and undesired interferences. Major SIW losses are related to dielectric and conductor

losses, therefore a good choice of the dielectric material and the conductor can reduce the contribution of these two losses. Surface roughness has also to be considered as the operating frequency increases at millimeter-wave frequencies.

II. Transition from SIW to other transmission lines

SIW is not a stand-alone component in the PCB, so it has to be integrated with other millimeter-wave or microwave components on the board. Therefore, one of the major challenges of this technology, is the design and characterization of the transition to other structures of transmission lines. Transitions from SIW to microstrip, CPW, RWG and directly to the chip are presented below.

A. SIW to microstrip transition

The first transition from the SIW to other transmission lines introduced, have been the SIW to microstrip transition, which is still one of the most used transitions for single-layer circuits. Fig. 2 show the structure of this transition which consists of three parts that are SIW part, microstrip part, and the taper section, which connects the microstrip line to the top wall of the SIW.

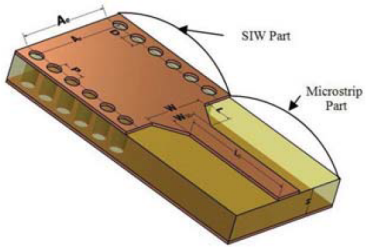

Fig. 2. Transition structure from microstrip line to SIW [5].

The taper converts the quasi-TEM mode of the microstrip to the TE_{10} mode which propagates into the SIW. The tapered section is designed so that an impedance match between the SIW and the microstrip line is achieved. Analytical expressions for the design of the microstrip taper are given in [6].

A new wideband transition from microstrip line to SIW has been reported in [7]. Two additional vias are added to the design of the transition, which are placed symmetrically at both sides of the microstrip taper. Compared to the microstrip taper, the additional vias forces the field to be more confined in the lateral direction, which leads to better matching between microstrip and the SIW. The performance of the new design have been compared with conventional microstrip taper over all frequency bands in the range 8.2 to 90 GHz and the proposed new design shows a return loss better than -30 dB in all the bands compared to conventional taper transition, which shows a return loss better than -20 dB. The insertion loss of the new transition is measured only in the frequency range 12 to 18 GHz and measured insertion loss of the back to back transition is 0.82 dB, which shows a good agreement with the simulated results.

B. SIW to coplanar waveguide

Transitions from SIW to coplanar waveguide (CPW) show high potential for the upper mmW spectrum due to the CPW's compatibility with current monolithic millimeter-wave integrated circuits (MIMICs) and with electrically thick substrates which have a height of more than one-sixth of a wavelength in the medium, for which microstrip transmission line would show leakage due to excited surface or substrate waves[8]:

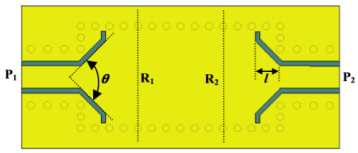

Fig. 3. A proposed transition from CBCPW to SIW [10]

A low loss ultra wideband transition between conductor backed coplanar waveguide (CBCPW) to SIW is presented in [10]. A linear tapper concept is presented and a design using a generalized impedance inverter is developed as shown in Fig. 3. The design shows very good results regarding the insertion loss and bandwidth. The added vias on both sides of the CBCPW increase the field matching between the two structures. The length and angle of the central tapered strip are optimized for impedance matching. An insertion loss of better than 0.4dB have been measured over the entire Ka-band and the return loss is better than 20 dB. Other transitions using current probes have been presented which are implemented in a very thick substrate or CPW to SIW transition however, the achieved bandwidth is smaller compared to the above-proposed design.

Based on the simulation results presented in Fig. 4 it can be concluded that for a GCPW-SIW transition the use of a substrate with a higher dielectric constant, increases the fractional bandwidth of the transition and a lower insertion loss can be achieved. However, an increase in the substrate thickness would increase the insertion loss caused by radiation. GCPW characteristic impedance is almost independent of the substrate thickness and shows similar value to SIW's characteristic impedance which results in good impedance matching between the two structures [9] which can be confirmed by the good simulation results of the return loss shown in Fig. 4.

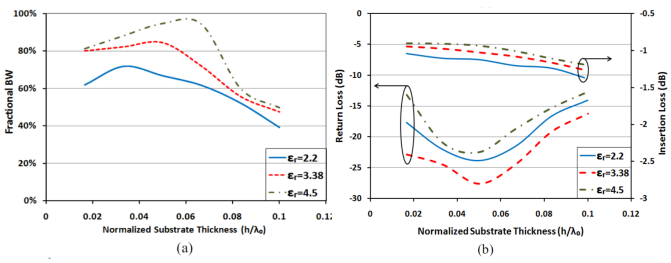

Fig. 4. Simulated (a) Fractional bandwidth and (b) return and insertion loss versus substrate thickness of a back-to-back GCPW-SIW transition [9].

C. A Transition from SIW to Rectangular Waveguide

The SIW-to-RWG transition has been investigated in many papers meanwhile, two main groups can be defined based on the transition geometry: a right angle configuration where the SIW and RWG are perpendicular to each other and an in-line configuration where the SIW and RWG have the same axis orientation. The in-line configuration is designed by using different methods such as finline taper, RWG-taper or by inserting a coupling probe inside the RWG.

Simple and compact transitions between SIW and the rectangular waveguide are proposed in [11-16], in which the RWG intersects vertically to the SIW structure. The coupling between the two structures is realized by a slot etched on the top layer of the SIW, which can convert the TE_{10} mode of the SIW to the TE_{10} mode of the RWG. Compared to the inline transition, the right angle transition show in general narrow bandwidth however, they offer a compact size and less manufacturing complexity. Some modifications have been presented in [11-12] to increase the bandwidth of the design, such as adding some additional inductive posts to the design in order to provide a better impedance matching between the SIW and the RWG. In [11] two electrical probes, realized by two posts are designed inside the coupling aperture to increase the conversion between the SIW mode and the rectangular waveguide mode. A two-step ridged waveguide coupled to the etched slot of the SIW is presented in [16]. The developed design presents a better field and impedance matching, therefore an operational bandwidth over the entire Ka-band can be achieved.

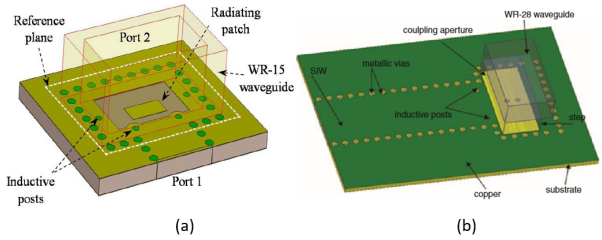

Fig. 5. (a) A proposed SIW to RWG right-angle transition [12], (b) Configuration of right-angle transition using electrical probes [11] .

Another method for designing the transition between SIW and RWG can be implemented by using a probe inside the RWG as shown in [17-18]. In [17] a broadband transition structure with compact size and low fabrication cost is realized by inserting an antipodal quasi-Yagi antenna probe into the center of the RWG as shown in Fig. 5c. In [18] a radial probe extended from an SIW is inserted into a height-tapered waveguide, however as shown in the graph in Fig. 7, if the probe is compared to other transitions it presents a wide bandwidth and short length but high losses which are more than 2.5 dB for this design. The use of probes, in general, complicates the design and the insertion loss increases up to values that may compromise the performance of the transition.

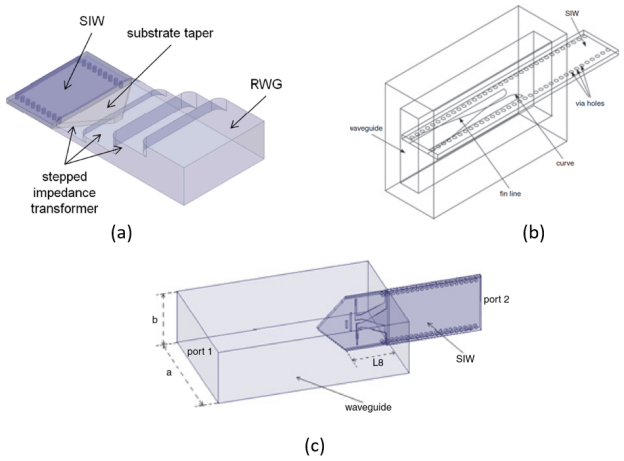

Fig. 6. (a) SIW-to-RWG transition structure using a RWG-taper [21], (b) Air-filled waveguide to SIW transition using finline-taper [23], (c) Waveguide to SIW transition using a probe [17].

Another transition from SIW to RWG can be performed by inserting a substrate taper into the stepped impedance transformer of the RWG as shown in Fig. 6a. The goal is to improve transmission loss and bandwidth of the transition. In [22] an inline air-filled waveguide to SIW transition which use a four-section height-stepped waveguide combined with a single-step widening transformer is presented. This design combines the bandwidth control capability with a simple scalable structure that avoids the use of probes for increasing the bandwidth and therefore keep a relatively low insertion loss which makes it adequate for successful use in millimeter wave frequency applications.
A 15dB bandwidth (S_{11} < -15 dB) of 49% over the frequency range 31-51 GHz with a measured back to back transmission loss of 0.8 dB is achieved for the presented design.

Another design that uses a finline taper as shown in Fig. 6b can be used to realize the transition from SIW to RWG. A way of improving the overall performance of the SIW-to-finline transition, is attained by adding an antipodal finline transition to the taper, which is inserted into the metal waveguide and works as impedance or waveform transformer. In [24] a SIW to rectangular waveguide transition with antipodal finline operating in Ka-band is presented which consist of two parts: one presents the SIW to an antipodal fin-line transition and the other is an antipodal to fin-line to a rectangular waveguide transition. The finline length has to remain short in order to avoid the increase of loss over the whole Ka-band. Based on the results shown in Fig. 7 the design presented in [25] shows high fractional bandwidth, low loss and a very short length. Having a small size, good bandwidth and very low losses compared to other transitions, make this design appropriate for integration in millimeter-wave communication systems, radar or measuring systems that use substrate integrated waveguides.

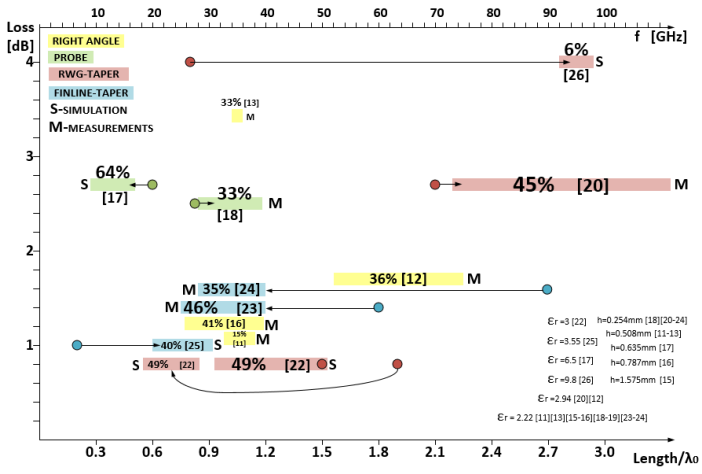

Fig. 7. SIW to RWG transition performance chart.

The graph, shown in Fig. 7, presents an overview of transition configurations from SIW to RWG. The 15 dB bandwidth (S_{11} < -15 dB) for each transition is taken from simulations results if no data for back to back transition measurement exists. The losses are taken from back to back measured values and the lengths are normalized to the free-space wavelength at the center frequency of each transition. Two relationships are presented in the graph. First the insertion loss versus the fractional bandwidth presented by the bars and second the loss versus the length of the inline transitions presented by the dots. In many papers a slight increase of the measured insertion loss compared to the simulated values is observed which can be related to the manufacturing tolerance effects of the SIW or the surface roughness, especially in the millimeter-wave range. A solution for reducing the loss caused by surface roughness would be the use of a substrate with a super polished metal surface.

D. Direct Transition from SIW to Chip

A new method of bonding the chip directly to the SIW is presented in [27]. The traditional way of integrating an IC chip with the SIW consist of first transforming the SIW to a microstrip line and then connecting the microstrip and the chip pad with a bondwire. However, such a transition increases the overall circuit size and can introduce extra loss.

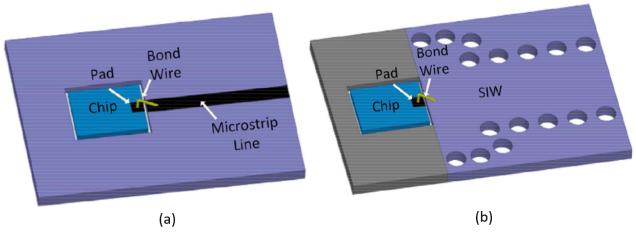

Fig. 8. (a) Wire bonding structure between chip and microstrip, (b) Wire bonding structure between chip and SIW [27].

Fig. 8b shows the proposed transition between IC chip and SIW. The bonding wire connects the chip pad with the top metal surface of the SIW. As the bonding wire presents some inductive effects in millimeter wave frequency range, a compensation structure is designed by expanding the distance between the two rows of vias close to the bonding wire, which adds a equivalent capacitance.
Fig. 9 show the simulation results of both structures. Return loss values better than 10 dB are achieved for both structures over the frequency range 76-80 GHz. The insertion loss (IL) of SIW Bonding is slightly better than the IL of the microstrip bonding, however for radar applications on the W-band, the IL is very high. An optimization of the bonding wire structure can improve the performance and reduce the insertion loss of the transition.

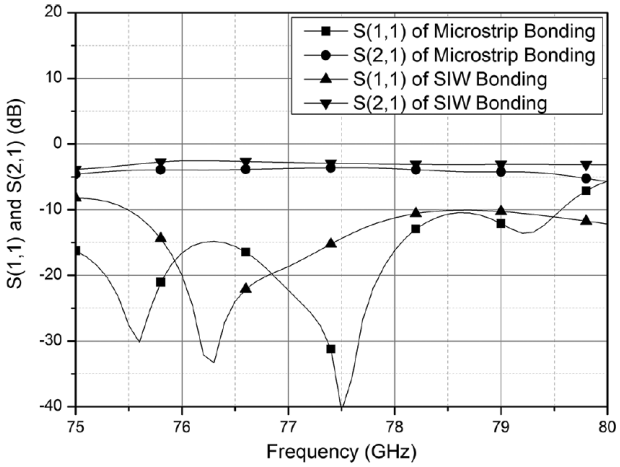

Fig. 9. Simulated results of microstrip compared to SIW bonding [27].

A good alternative to replace the bondwire would be flip-chip. Today most of the chips used in automotive radar at 77 GHz are flip-chip and a transition from SIW to the flipped-chip, could show promising results regarding the losses. However, to the author best knowledge there were no investigations of such a transition reported, therefore this remains a topic of future research.

III. Conclusion

This paper presents an overview on substrate integrated waveguide transitions, which enable the connection between planar and nonplanar components with substrate integrated waveguides. Many efforts have been made recently to design high performance and robust transitions from SIW to microstrip line, CPW, and RWG. The attempts made by using different transition methods, to improve the performance of the SIW regarding the bandwidth and loss are investigated. Some future research has to be made in order to design a direct transition from SIW to chip with very low losses, which can open new application areas for the SIW.

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Temperature Sensitive Electrical Parameters in SiC Power MOSFETs

Tanumita Haldar
Electrical Engineering (MSc.)
University of Stuttgart
Stuttgart, Germany
st169673@stud.uni-stuttgart.de

***Abstract*—The measurement of junction temperature using Temperature Sensitive Electrical Parameters in Silicon Crabide Metal-Oxide-Semiconductor Field-Effect-Transistor(SiC MOSFET) is challenging due to faster switching speed and lower sensitivity because of wide band-gap eneR_Gy. The paper illustrates the following thermo-sensitive electrical parameters of SiC Mosfet: Conduction Voltage V_{DS},on (static), Threshold Voltage V_{th}, Internal Gate Resistance $R_{G,int}$, Transient Switching Behaviour di_{DS}/dt, Turn off delay time td,off, The TSEPs are also compared with respect to various criteria like sensitivity, linearity, generality, etc. The optimal TSEP for SiC MOSFET has also been proposed.**

***Index Terms*—SiC MOSFET, temperature measurement, temperature sensitive parameters, wide band gap devices**

I. Introduction

The condition monitoring of the power semiconductor devices is essential to ensure the state of health of the device during its field operation. The measurement of junction temperature of a power semiconductor device can be used to characterize thermal performances of its package and to indicate damage of the power module. The three methods to measure temperature in semiconductors:

1. Optical
2. Physically Contacting
3. Electrical

Sensor-less online junction temperature measurement are used because some in-built characteristics of semiconductors offer unique capability to measure temperatures without direct mechanical or optical contact and also we are able to measure the temperature during fast switching transients. The temperature measurement of SiC Mosfet using TSEPs comes into picture because there is a known relation between TSEP and temperature.Further, using TSEPs is challenging in SiC due to faster switching transients and lower sensitivity to temperature due to wider band-gap. List of TSEPs to be considered:

- Conduction Voltage $V_{DS,on}(static)$
- Threshold Voltage V_{th}
- Internal Gate Resistance $R_{g,int}$
- Transient Switching Behaviour dI_{ds}/dt
- Turn off delay time $T_{d,off}$

II. Temperature sensitive parameters

A. Conduction Voltage $V_{DS,on}$

The ON-state resistance $R_{DS,on}$ and the forward conduction voltage $V_{DS,on}$ have quite a good sensitivity to temperature as shown in the measurements in Fig. 1 [2]. But the temperature dependence is potentially nonlinear and current-dependent; therefore, its use in online monitoring requires decoupling of the load. $V_{DS,on}$ is also dependent on the state-of-health of device. The main problem in the practical use of $V_{DS,on}$ for online monitoring is the significant voltage excursion across drain–source terminals during converter switching, ranging from few Volts during conduction to well over the dc-link voltage V_{dc} during turn-OFF transients. The emitter–follower circuit illustrated in Fig. 1 shows a solution to the measurement of $V_{DS,on}$ of the device M1 under test. When Drain D voltage rises above a reference voltage (here 9V)[2], device M2 isolates the circuit from high voltage side during turn-OFF transient of M1. V_m is limited to a safe level now. When M1(DUT) is turned on, $V_{DS,on}$ is low and M2 is saturated. Thus, the voltage V_m across R is equal to $V_{DS,on}$.

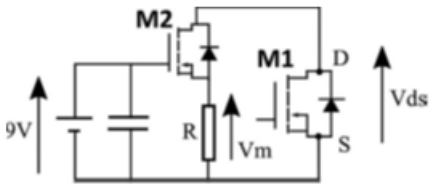

Fig. 1. Circuit schematic for $V_{DS,on}$ measurement

B. Threshold Voltage V_{th}

The threshold voltage V_{th} is the minimum gate–source voltage required to switch ON the device.

The increase of carrier concentration and the decrease of bandgap with temperature result in a decrease of V_{th} with temperature. It has been reported that as T_j increases, V_{th} of SiC MOSFET decreases [6]. V_{th} is measured by sensing gate voltage directly at the beginning of current rising. However, the switching speed of SiC MOSFET is very high and there may be resonance at the V_{gs} waveform, making the V_{th} hard

to be detected. A suitable method used for the detection of a quasi-threshold voltage is shown in Fig. 2 [2]. A voltage across the parasitic inductance between the auxiliary Kelvin source (S') and the source (S) is generated when the device current i_{DS} starts to rise during device turn-ON. The rising edge of the voltage $V_{SS'}$ across the parasitic inductance, which is proportional to di_{DS}/dt, can be used to trigger the sample and hold circuitry acquiring the gate–source voltage $V_{GS'}$ effectively capturing the start of conduction and therefore the quasi-threshold voltage. In [4], V_{th} was also calibrated at different T_j varied from 25°C to 180°C. Fig. 3 shows results. Beyond 80°C V_{th} has a negative temperature coefficient as about -9mV/°C, which is adequate enough to sense the T_j.

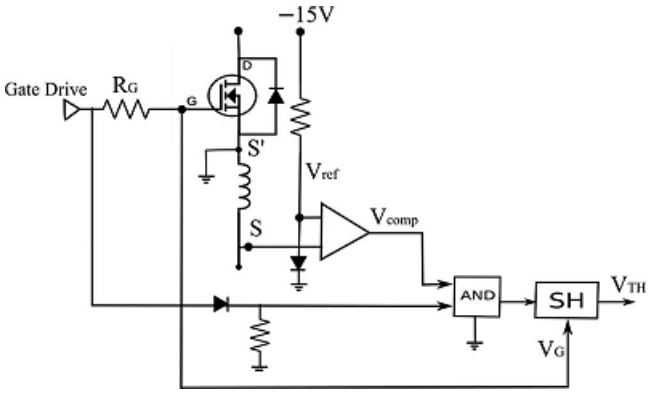

Fig. 2. Schematic circuit for quasi-threshold voltage measurement

C. Internal Gate Resistance ($R_{G,int}$)

The internal gate resistance $R_{G,int}$ is the lumped equivalent of the distributed resistance of the polysilicon gate and metal contacts in the MOSFET device. $R_{G,int}$t can be considered in series with the parallel of the gate–source and gate–drain capacitances. The time constant T_{on} of the equivalent gate capacitance cha$R_G$ing process during turn-ON before V_{th} is reached and can be expressed as :

T_{on} = ($R_{G,ex}$ + $R_{G,int}$) (C_{GS} + C_{GD} (V_{DS}))

where $R_{G,ex}$ is the external gate resistance, C_{GS} and C_{GD} are the gate–source and gate–drain capacitances, respectively. At turn-ON, for a fixed dc-link voltage, the drain–source voltage V_{DS} can be taken constant; hence, C_{GD} can also be considered constant. C_{GS} does not change significantly until V_{th} is reached. $R_{G,ex}$ is assumed to be constant at a known ambient temperature. It is evident that $R_{G,int}$ becomes the dominating temperature-dependent parameter in the equation affecting gate current during turn-ON. The peak of the gate current iG can be considered proportional to $R_{G,int}$. The internal gate resistance is measured using a peak detector circuit whose peak is directly proportional to the gate current which in turn is proportional to the internal gate resistance and is shown in Fig. 4 [2]. Similar to V_{th} , the internal gate resistance as TSEP is potentially load independent. Heavy doping of polysilicon required for low resistivity gates typically results in low temperature coefficient of its resistivity, potentially resulting in low sensitivity of $R_{G,int}$ as a TSEP. The advantage of using a peak detector circuit is that there are no additional control signals required and it can be applied across a wider range of device sizes.

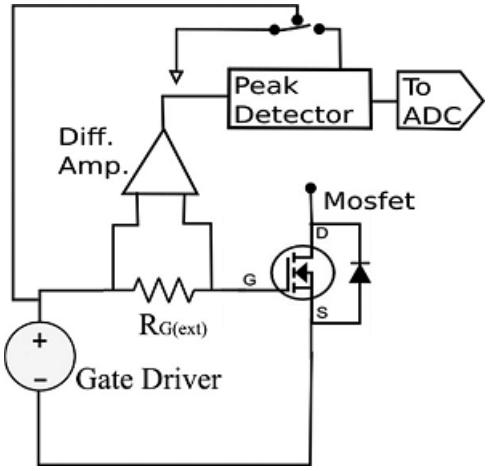

Fig. 4. Schematic circuit for gate current peak detection.

D. Turn-On Transient (di_{DS}/dt)

The rate of change of device current i_{DS} during a turn-ON transient can be expressed as:

di_{DS}/dt = uC$_{OX}$ $\frac{W}{L}$(V_{GS}-$V_{th}$$V_{GG}$/($R_G$($C_{GS}$+$C_{GD}$)) e$^{-t/(R_G(C_{GS}+C_{GD}))}$

where u is the electron mobility, C_{OX} is the intrinsic gate oxide capacitance, W/L is the gate width/length ratio, and V_{GG} is the gate drive voltage. The negative temperature coefficient of both threshold voltage V_{th} and mobility has contrasting influence on di_{DS}/dt . The di_{DS}/dt increases with rise in temperature due to the negative temperature coefficient of threshold voltage. di_{DS}/dt increases with increase in temperature and rising intrinsic carrier concentration as more carrier ions flow through the channel. Hence, di_{DS}/dt exhibits a positive temperature coefficient. Since the voltage $V_{SS'}$ across the source parasitic inductance $L_{SS'}$ is proportional to the rate of change of i_{DS}, the peak value of $V_{SS'}$ will be used as an indirect measurement of as illustrated in Fig. 6. The integration of $V_{SS'}$ can be used to estimate the output current i_{DS} as illustrated in the setup in Fig. 5 can provide a practical way of estimating device current which can be used to decouple load and temperature dependence of the proposed TSEPs.

The di_{DS}/dt can be obtained by Equation [7]:

di_{DS}/dt = Vs's/L$_s$

The junction temperature can be obtained in real time by using equation :

T= K$_0$($V_{s's}$–$V_{s's}|_{T0}$) + T_0

where K_0 is the temperature resolution and $V_{S'S}|_{T0}$ is the $V_{S'S}$ value at temperature T$_0$.

E. Turn OFF Delay time (t_{d_off})

Turn-off delay time is defined as the interval between the moment when the gate-source voltage starts to decrease and the moment when the drain-source voltage begins to increase.

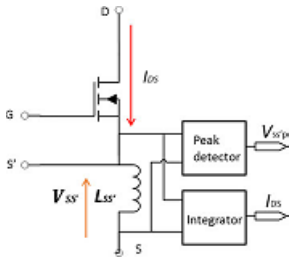

Fig. 5. Schematic circuit for measurement of peak voltage and current across $L_{SS'}$

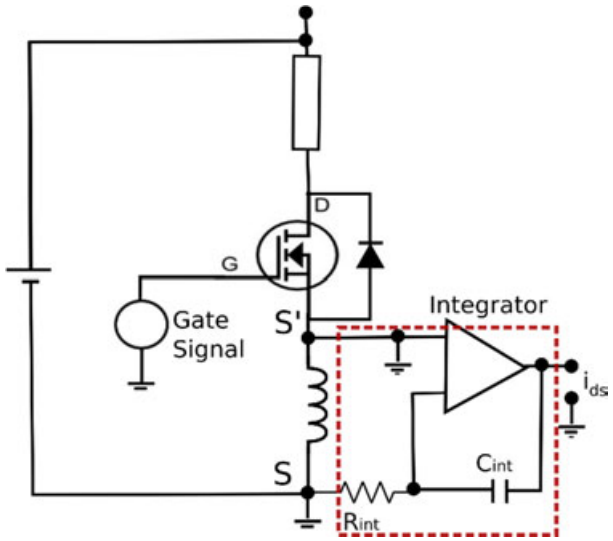

Fig. 6. Current measurement using integration of $V_{SS'}$

Fig. 7 illustrates a typical transfer characteristic of a 1200-V/24-A SiC MOSFET and its dependence on temperature [5]. It shows that Miller voltage changes as junction temperature varies. Hence, the turn-off delay time is temperature dependent.

The turn-off delay time can be expressed as a function of gate drive, operating current, and junction temperature.

Fig. 8 illustrates the turn-off delay time $t_{d,off}$ dependence on junction temperature Tj under different operating voltages V_{DC} with a 1200-V/24-A SiC MOSFET.

Fig. 9 illustrates the turn-off delay time $t_{d,off}$ dependence on junction temperature Tj under different operating currents IL. It shows that the sensitivity is extremely small mainly due to the small input capacitance of SiC devices together with the limited gate resistance for fast switching.

III. Comparison of TSEPs consdering different criteria

It would be an interesting approach to compare and observe the different TSEPs considering different criteria and the conclude the optimal TSEP. The paper includes four comparison criteria : sensitivity, linearity, generality and calibration needs.

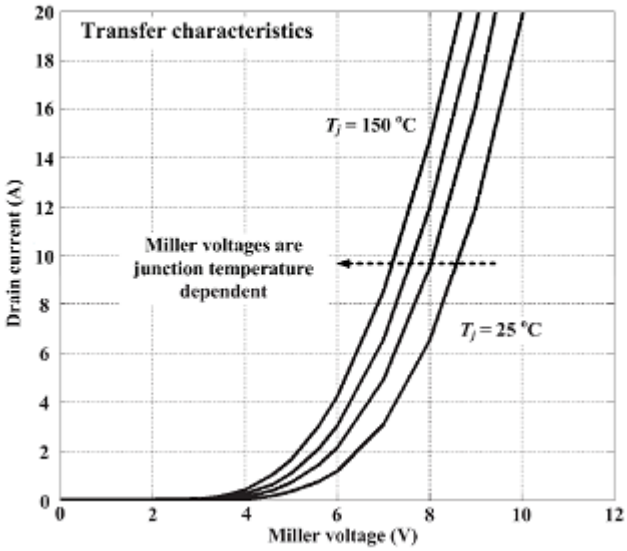

Fig. 7. Transfer characteristics vs. junction temperature.

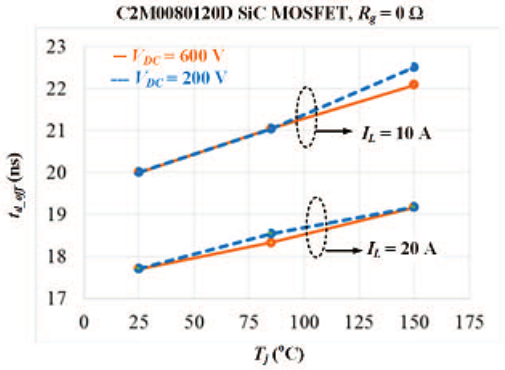

Fig. 8. Sensitivity dependence on DC bus voltage V_{DC}.

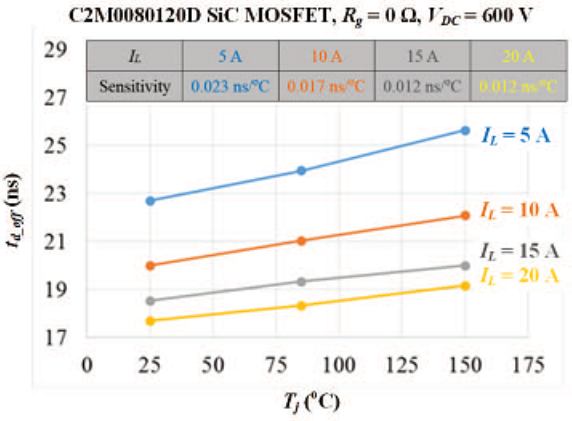

Fig. 9. Sensitivity dependence on load current I_L.

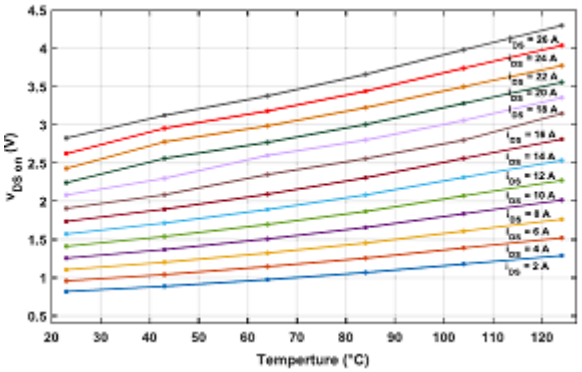

Fig. 10. Measured oN-state voltage V_{DS} on as a function of temperature and load current

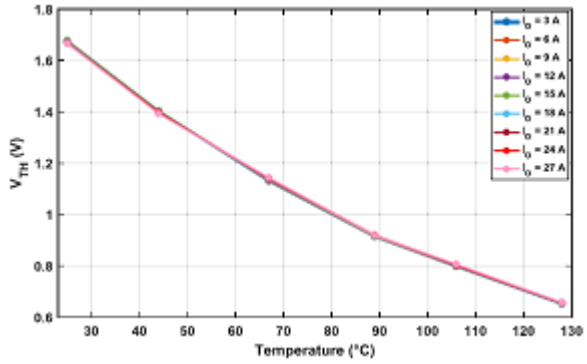

Fig. 11. Measured quasi-threshold voltage versus temperature and load current

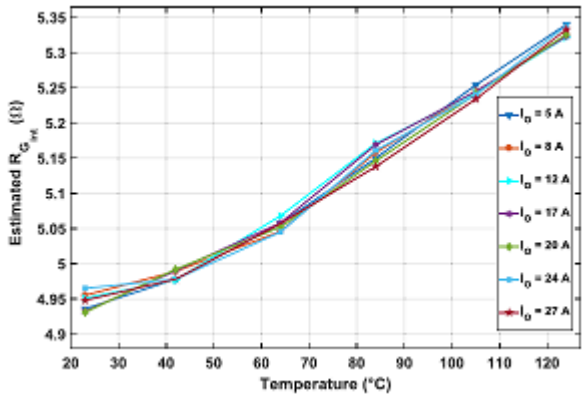

Fig. 12. Measurement of the estimated internal gate resistance as a function of temperature and load current

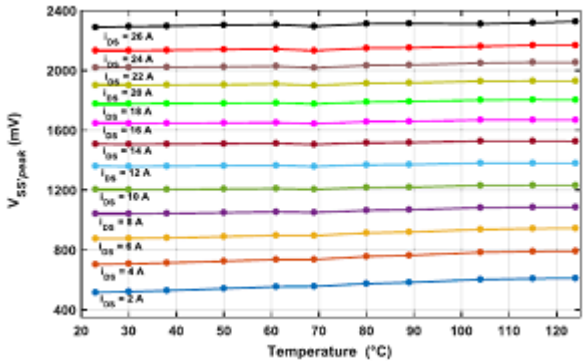

Fig. 13. Measured peak voltage V_{SS} peak over parasitic source inductance as a function of temperature and current

A. Sensitivity

Other than temperature measurement during the switching time, all TSEPs are voltage measurements. The measured ON-state voltage V_{DS},on as function of temperature and load current with V_{GS} = 20 V is shown in Fig. 10. A good sensitivity of 13.7 mV/∘C at maximum current is demonstrated, similar to the sensitivity of approximately 10 mV/∘C reported in the device datasheet using offline methods. There could be a small deviation due to difference in testing conditions, e.g., gate drive voltage and device variability. The voltage under a high current may not be the best case. Further, unlike other TSEP, this parameter is strongly dependent on the test conditions. The measured quasi-threshold voltage as a function of temperature and load current is shown in Fig. 11. The expected negative temperature coefficient of V_{th} is confirmed. Good sensitivity of 9.3 mV/°C is shown. However, the sensitivity value of switching delay (turn -on/turn-off delay) is very low and does not permit an easy accurate temperature measurement The estimated internal gate resistance as function of temperature and load current is shown in Fig. 12. Relatively small sensitivity of 3.6 m/∘C makes the method potentially sensitive to noise. Fig. 13 illustrates the measured peak voltage $V_{SS'}$ variations with temperature and load current across the parasitic inductance between source and auxiliary source connection. This voltage is a signal proportional to di_{DS}/dt. A very low sensitivity to temperature variation is visible, thereby making it difficult to use as TSEP. Turn-off delay time has a low sensitivity to temperature. With a gate impedance regulation assist circuit, the sensitivity of turn-off delay time on junction temperature can be increased with little penalty of the power conversion performance.

B. Linearity

The linearity is an interesting indicator for the data processing. It is also important for the calibration step because a linear TSEP does not need a lot of measurement points. A good linearity with temperature is also evident in case of conduction voltage V_{DS},on. The measured quasi-threshold voltage as a function of temperature and load current is shown in Fig. 10. A relatively good linearity is observed. The estimated

internal gate resistance as function of temperature and load current is shown in Fig. 11. A good linearity with temperature is demonstrated. Turn-off delay time is a typical TSEP with excellent linearity and ruggedness.

C. Calibration needs

Every TSEP needs a calibration step. Still, this procedure can be more or less long if a TSEP is chosen instead of another. In fact, the linearity could reduce the measurement points number as mentioned earlier. Furthermore, a TSEP value can be different from one chip to another having the same reference and the same temperature. The ON-state voltage is current-dependent and therefore the use of V_{DS},on as TSEP requires an independent measurement of device current in order to decouple the load from temperature effects. The threshold voltage is invariant to load current. A good load invariance is observed in case of internal gate resistance (R_G,in). Temperature variation in external gate resistance and in the gate drive circuit will also affect the accuracy of estimation. Therefore, the external gate resistance should be selected with very low temperature coefficient. The voltage variation due to load current is more significant in turn-on transient.

D. Generality

The use of di_{DS}/dt as TSEP is promising for applications where a high switching rate is not required. The temperature sensitivity of both the maximum di_{DS}/dt and di_{DS}/dt at low V_{GS}, in the vicinity of V_{th}, can be used. This parameter is more suitable for high current rated devices.

CONCLUSION

Conduction voltage, switching delay, internal gate resistance, turn-on transient and threshold voltage have been considered to illustrate their potential to measure the junction temperature of SiC MOSFET. The conduction voltage and the quasi-threshold voltage show a good sensitivity to temperature while all the parameters have good linearity. While the on-state voltage has a load variance, both threshold voltage and internal gate resistance are load invariant. The voltage variation due to load current is more significant in turn-on transient. From the discussions, we can conclude that among the above-mentioned TSEPs, quasi-threshold voltage can be considered the optimal TSEP to measure the temperature in SiC MOSFET devices.

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Analog Pre-Distortion for mmW-Amplifiers

Thomas Ufschlag
Institute of Robust Power Semiconductor Systems (ILH)
University of Stuttgart, Germany
st170231@stud.uni-stuttgart.de

***Abstract*—An investigation of different analog pre-distortion concepts for millimeter-wave amplifiers has been conducted based on published research. Common linearity figures of merit like the third order intercept point and the 1-dB compression point are introduced. The different system level approaches for power amplifier linearization are presented and compared. The concepts of all investigated papers are briefly summarized and also compared among each other regarding their key properties. Finally, the suitability of the discussed concepts for millimeter-wave monolitic-integrated-microwave-circuits (MMIC) is judged and a conclusion is provided.**

***Index Terms*—analog pre-distortion, linearization techniques, linear amplifier, mmW amplifier, MMIC, pre-emphasis, efficiency improvement**

I. Introduction

Radio frequency (RF) power amplifiers (PA) in transmitters for millimeter-wave (mmW) must meet the requirements of linearity and efficiency [1, p. 1]. Millimeter-wave refers to the used frequency range of 30–300 GHz.

The nonlinear transfer characteristic (TC) of a PA leads to intermodulation (IM) products and harmonics [1, p. 7 ff.]. Fig. 1 shows the output spectrum of a PA, which has quadratic as well as cubic components present in its TC and generates thus IM products of second and third order [1, p. 8 ff.]. The IM products depict in Fig. 1 are produced by applying the two closely spaced fundamental tones ω_1 and ω_2 with equal amplitude at the input of the PA [1, p. 9]. These IM products are undesirable for a PA and hence they can be called intermodulation distortion (IMD) and harmonic distortion, respectively. The IMDs at $2 \cdot \omega_2 - \omega_1$ and $2 \cdot \omega_1 - \omega_2$ are especially critical because they are close to the fundamental tones and thus hard to eliminate by means of a bandpass filter [1, p. 10].

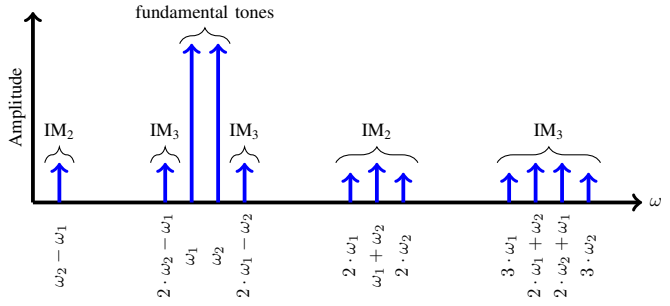


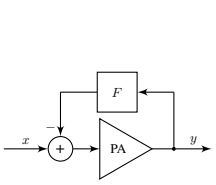
Fig. 1: Output spectrum of a nonlinear PA [1, p. 10], assuming that only second and third order nonliniearities are present in the transfer characteristic of the PA.

As described in [1, p. 8 ff.], with increasing input power of a PA its efficiency decreases due to the unwanted IM products. Efficiency is a performance metric for PAs which describes how much DC power is converted to RF output power [1, p. 16].

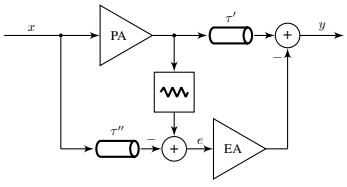
Figures of merit for linearity performance are the third order intercept point (TOI), also denoted as intercept point third order (IP3), which compares the power of two fundamental tones with the power of the third order distortion products [2, p. 2]. By convention, the IP3 for high-gain devices like PAs is output related (OIP3) and for passive devices like mixers input related (IIP3) [2, p. 4]. Furthermore, there is the 1-dB compression point ($P_{1\,\mathrm{dB}}$) [3, p. 513]. The 1-dB compression poin gives an input ($P_{1\,\mathrm{dB,\,in}}$) or output ($P_{1\,\mathrm{dB,\,out}}$) related power level, where the ideal linear and actual nonlinear TC of the PA deviates by 1 dB [3, p. 513]. The Adjacent Channel Power Ratio (ACPR) is another important linearity metric, which describes the ratio of the power in a carrier channel relative to the adjacent channel [2, p. 9]. The amplification of a modulated wideband signal with means of a nonlinear device will lead to spectral re-growth [2, p. 9]. The spectral re-growth then leaks into an adjacent channel and can be measured by the ACPR [2, p. 9].

The highest efficiency of a PA can be achieved if it is operated close to saturation [4], [5]. But this operating point (OP) inherently leads to signal distortions [4], [5]. A simple approach to avoid the distortion caused by nonlinearites of a PA is to operate at a lower average output power [1, p. 2]. This technique is referred to drive the PA in a certain amount of back-off [1, p. 2]. Today's wireless communications achieve their high data rates due to more complex modulation formats and a higher bandwidth (BW) [6], [7]. The complex modulation formats show higher amplitude peaks because more signals are modulated onto a signal [1, p. 1]. This results in a high peak-to-average-ratio (PAR) [1, p. 1]. Maintaining linearity of a PA with the back-off-technique is not desirable, because high PAR signals require to shift the OP further away from saturation and consequently compromises the efficiency of the PA [1, p. 2].

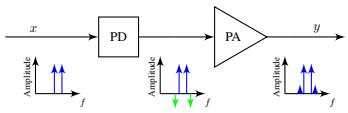
There are two solutions which simultaneously achieve high efficiency and good linearity [1, p. 2]: PAR reduction, also known as crest factor reduction, which allows the PA to operate at higher average output level by modifying the waveform with means of digital signal processing (DSP) and PA linearization which linearizes the TC of the PA [1, p. 2 f.].



(a) Feedback [1, p. 20].



(b) Feedforward [1, p. 20].



(c) Pre-Distortion [1, p. 21].

Fig. 2: System Level Approaches for PA linearization.

II. System Level Approaches for PA Linearization

A. Feedback Technique

The FB technique, shown in Fig. 2a, is the simplest technique to reduce IMDs [1, p. 19]. On the downside, the electrical delays around the feedback loop limits the BW of signals which can be corrected [1, p. 19]. The BW of signals which can be corrected will be further on referred to as the Correction BW (CBW).

B. Feedforward Technique

Fig. 2b depicts the FF technique, which achieves a better IMD suppression because loop delays are not present [1, p. 19]. The drawback is the more complicated realization which requires for e.g. an error amplifier (EA) which can itself produce distortion products in the output spectrum [1, p. 19]. Besides that, since there is no closed loop architecture, it's impossible to take changes regarding device characteristics trough ageing and temperature into account [1, p. 19 ff.].

C. Pre-Distortion Technique

In Fig. 2c the principle function of the PD technique can be seen. PD cancels out the IMD by generating a distortion, which is precise the contrary to the distortion caused by the PA [1, p. 20]. The PD block is pre-connected to the PA and has to generate the exact equal amplitude with out-of-phase to cancel the IMD completely [1, p. 21]. PD is performed a priori and can in principle cancel out all IMD products like the third, fifth, seventh and and all other odd order IMD products [8]. With this technique, a wide BW can be corrected [1, p. 21].

D. Comparison

Table I provides an overview of the mentioned techniques for PA linerarization. It is striking that PD provides a moderate performance regarding IMD cancellation with the advantage of a medium to high CBW, simple circuit configuration and especially a low power consumption [1, p. 21]. Due to this facts, PD seems to be a suitable solution for handset mmW-MMIC-based linearizers.

Table I: Comparison of the System Level Approaches [1, p. 22].

Technique	Distortion Cancellation	BW	Efficiency	Size
Feedback	Low	Low	Medium	Medium
Feedforward	High	High	Low	Large
Pre-Distortion	Medium	High/Medium	High	Small

III. The Need for Analog Pre-Distortion (APD)

Digital pre-distortion (DPD) has been widely used for macro-cell base stations over the last decade, where power consumption is not the decisive aspect [1, p. 3]. The main problem with DPD in regard to the recent demands is, that the sampling frequency must be significantly higher than the desired CBW [9]. To suppress up to the fifth order IMD, the clock speed must be five times higher than the CBW [1, p. 23].

APD has the advantage that it can be implemented with negligible power consumption compared to DPD [10]. This is especially important for battery powered devices [1, p. 1]. On the other hand, DPD has shown superior performance compared to APD [1, p. 3]. DSP is faster, more accurate and more flexible than analog signal processing (ASP) [1, p. 3].

Summary of the issues of DPD for mmW-MMIC:

- Extreme high clock speed is mandatory to avoid aliasing effects and leads to high power consumption and system complexity [1, p. 23]
- DSP itself consumes to much power for battery powered applications [1, p. 23]
- Size not suitable for MMIC [1, p. 23]

ASP can not outperform DSP as mentioned in [1, p. 5]. But due to the listed issues, research and consequently this paper focuses on analog realization of the system level approach PD. The overall target is to find APD solutions, which provide adequate performance. The additional advantages of APD like lower complexity, lower power consumption and more compact design are especially crucial for low power MMIC applications [1, p. 5].

To meet the requirements of future communication systems, research in the field of APD has to be conducted.

IV. Published Concepts of Analog Pre-Distortion

A. A New Envelope Pre-Distortion Linearization Architecture for Handset Power Amplifiers

The researchers in [11] simulate a new envelope PD architecture, which combines the FB and PD approach [11, p. 175].

With log amps and phase detectors, the instantaneous complex gain of input and output are estimated [11, p. 175]. Due to feedback of the information about amplitude and phase of the output signal to a voltage controlled variable attenuator and a phase shifter, amplitude and phase distortion can be eliminated [11, p. 175].

The result of the simulations indicate that IMD suppression of more than 20 dB can be achieved with a BW of 1.2888 MHz with commercial available analog integrated circuits [11, p. 175]. The used center frequency of the cdmaOne singal was 881.5 MHz [11, p. 178]. According to the authors of the paper, the proposed architecture could be integrated on a single chip

with DC power consumption suitable for mobile applications [11, p. 175].

B. Analog-Controlled Feedback for Pre-Distortion of GaN PA

In paper [12], a simulation of an analog-controlled feedback for PD of a GaN MMIC PA for X- to Ka-band is presented [12]. The researchers mainly focus on reducing the PAR for switched mode PAs by means of delay control [12].

The researchers propose a simple first order passive filter as feedback with variable conductivity (e.g. MOSFET or HEMT) for delay control [12]. The conductivity in the loop filter is tuned by the PAR estimation scheme which calculates the peak allocation [12].

Controlling the output power and correct the TC with the feedback based on delay provides minimization of PAR by means of analog stabilization of conversion time delay [12]. The result of the analog-controlled feedback is a compensation of up to $2\,\mathrm{dB}$ of the gain error by losing less than $1°$ of phase error [12].

C. Linearization of Subthreshold Low-Noise-Amplifier (LNA)

The scientists in [13] present a LNA consisting of a cascode, where the transistors are biased in the subthreshold region [13, p. 377]. The LNA is designed for a center frequency of $2.4\,\mathrm{GHz}$ and is made of $0.13\,\mu\mathrm{m}$ CMOS technology [13, p. 377].

The reason for choosing an operation point in the subtreshold region is the higher transconductance to drain current [14]–[16]. The problem in the subtreshold region is the limited linearity [13, p. 377]. Common linearization methods use the transistors biased in strong inversion, where the linear gain and third-order nonlinearity coefficient have opposite signs [17]. If CMOS transistors are operated in the subthreshold region, the linear gain and third-order nonlinearity coefficient have the same signs [17]. Hence the researches provide a novel technique for subthreshold linearization [13, 377]. Only two additional parts are used for linearization: A capacitor and an inductance [13, p. 379].

The achievement of the suggested design is an improvement of the IIP3 by $11.2\,\mathrm{dB}$. For the proposed method, there is no auxiliary amplifier circuit needed [13, p. 380]. This results in a DC power consumption of only $240\,\mu\mathrm{W}$ for the whole LNA [13, p. 380].

D. 35–39 GHz CMOS Linearized Receiver with 2 dBm $IIP3$ and 16.8 dBm $OIP3$ for the 5G Systems

In paper [18], a 35–39 GHz linearized differential in-phase and quadrature components receiver is introduced, fabricated in 65-nm CMOS and finally its performance is tested [18, 92]. The scientist use a multi-gate transistor (MGTR) for PD [18, 92].

The RF amplifier consists of three common-source amplifiers with source degeneration inductors and a MGTR linearizer [18, 93]. The nonlinearized and linearized modes can be choosen by applying a different gate bias voltage at the certain gate of the MGTR transistor, which is located at the output stage of the amplifier [18, 93]. In the linearized mode, 3rd order transconductances of the MGTR output stage are cancelled [18, 93].

According to measurements, in linearized mode the gain is 15.5–$18.2\,\mathrm{dB}$ at 35–40 GHz [18, 93]. At 37 GHz, the $\mathrm{P}_{1\,\mathrm{dB}}$ is reached at $-10.6\,\mathrm{dBm}$ input power [18, 93]. The IM_3 power in linearized mode gets suppressed by 10–$16\,\mathrm{dB}$ compared to normal mode in the input power range from -30 to $-20\,\mathrm{dBm}$ [18, 93]. The PAs DC power consumption is $30.5\,\mathrm{mW}$ [18, 93].

E. A 6–16 GHz Linearized GaN PA

Paper [19] discusses the development of a MMIC chip consisting of a linearizer based on APD and a high power GaN amplifier [19, 1364]. Distortion correction is provided from 6–16 GHz [19, 1364 f.].

For applications which require a BW greater than one octave, its important to consider odd-order distortion products and also additionally even-order distortion products [19, 1364]. The even-order IMDs, especially the second HDs ($2{\cdot}\omega_1$, $2{\cdot}\omega_2$), the sum ($\omega_1 + \omega_2$) and the difference products ($\omega_2 - \omega_1$) can be reduced by using a push-pull-structure [20]. The push- and pull-structure is applied for the linearizer and the PA [19, 1364]. The linearizer consists of two active FET nonlinear generators (NLG), which are made of GaN HEMT devices [22]. One NLG is placed in the push-path, the other in the pull-path [19, 1364].

The MMIC PA-stage can deliver $10\,\mathrm{W}$ with a gain greater than $10\,\mathrm{dB}$ over the frequency range of 6–16 GHz [19, 1365]. The linearization method moves the $\mathrm{P}_{1\,\mathrm{dB}}$ $6\,\mathrm{dB}$ closer to saturation while the phase change is reduced from over $25°$ to less than $10°$ [19, 1365]. According to measurements of the authors, the push-pull-design of the linearizer results in at least $35\,\mathrm{dB}$ suppression of the HD_2 in the carrier power range from -20 to $-5\,\mathrm{dBm}$ [19, 1367]. They state a similar improvement for the push-pull-stage of the PA [19, 1367]. In the PAs linearized frequency range of 6–16 GHz, a minimum enhancement of the carrier-to-intermodulation of $8\,\mathrm{dB}$ and an increase in usable output power of more than $2\,\mathrm{dB}$ were achieved [19, 1367].

F. An E-Band Analog Pre-Distorter and PA MMIC Chipset

In paper [23] a MMIC chipset, consisting of an APD and a PA has been designed to improve the overall linearity for wireless communications in E-band [23, 31]. The E-band has allocated frequency ranges between 71–76 GHz and 81–86 GHz [24]. The scientists use a commercial available $0.1\,\mu\mathrm{m}$ InGaAs pHEMT technology [23, 31].

The APD circuit consists of two branches as shown in Fig. 3 [23, 32]. One linear branch, which is a fixed delay line used to match the delay caused by the other, nonlinear branch [23, 32]. A Class C EA is used in the nonlinear branch to produce a cubic term for IM_3 cancellation [23, 32]. A variable delay line (VDL) is used for phase control [23, 32]. The two branches get divided and combined by a $3\,\mathrm{dB}$ Wilkinson power divider and combiner, respectively [23, 32].

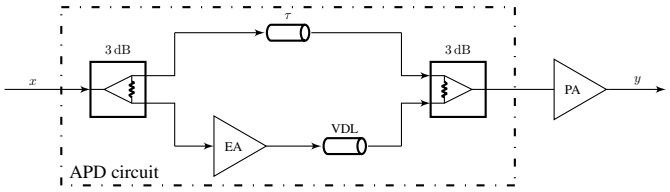


Fig. 3: Block Diagram of the APD circuit with post-connected PA [23, p. 31].

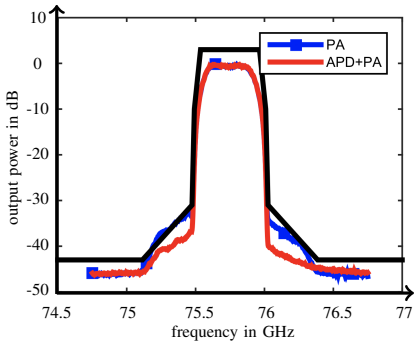


Fig. 4: Output spectrum of the MMIC chipset with and without applied PD [1, p. 33].

The result is an increase in the $P_{1\,dB}$ from $24\,dBm$ to $26\,dBm$ [23, 32]. The phase error in compression is reduced by approximately $3°$ [23, 32]. The linearization improves the carrier to IM_3 per tone at $18\,dBm$ up to $20\,dB$ [23, 32]. The practical application of the improvements is shown with a 64-QAM modulated signal with $250\,MHz$ modulation BW at $17\,dBm$ average output power [23, 33]. The center frequency is $75.75\,GHz$. An improvement in the ACPR of $5\,dB$ is achieved [23, 33]. The measured output spectrum is shown in Fig. 4, where the blue curve shows the spectrum of the nonlinearized PA and the red curve depicts the spectrum of the predistorted PA. The black mask follows ETSI EN 302-217-2 [23, 33]. The sprectral re-growth gets suppressed by means of the applied PD in order to meet the requirements of the given mask.

The downside of the linearization is that the insertion loss of the PD circuit reduces the small signal gain from $26\,dB$ by almost $8\,dB$ [23, 32].

V. Suitability of the Presented Concepts for mmW-MMIC

Table II provides an overview about the investigated papers and compares them among each other regarding key properties for mmW-MMICs, which will be named Key Performance Indicators (KPI) in the following. The most important KPI to judge if a concept is suitable for mmW-MMIC besides the sizes of the circuit is first of all the usable frequency range. The usable frequency range contains information about the CBW and the center frequency. The second important KPI is the overall DC power consumption, which compromises the efficiency of a PA. All the presented methods of the papers are sized for integration in a MMIC, hence size is not directly included in Table II. But from the circuit complexity, conclusion on the size can be drawn. It's again important to state that the feasibility of producing the circuit is given for all the presented methods, except the one from [12] which is just a theoretical paper.

Table II: Comparison of the presented concepts.

Paper	Freq.	BW	IMD Cancellation	Circuit Complexity	Power Consumption
[11]	Low	Low	High	High	Med.
[12]	Med.	n/a	High	High	n/a
[13]	Med.	Low	Med.	Low	Low
[18]	High	Med.	High	Med.	Med.
[19]	Med.	High	Med.	Med.	Med.
[23]	High	Med.	High	Med.	Med.

According to Table II, only the methods presented in [18], [23] are directly suitable for mmW-applications due to the capability of processing frequencies over $30\,GHz$. As stated in the table, this methods are also the only one which provide a high IMD cancellation with a relatively simple circuit approach. The techniques in [13], [19] might be adaptive for using mmW. The extreme high BW of the LNA presented in [19] has to be emphasized. On the downside, the high BW of this approach requires suppression of even-order distortion products and hence a more complex circuit than the methods from papers [13], [18].

Regarding on complexity, the circuit introduced in paper [13] is the simplest one. The presented linearized LNA has also shown a superior performance regarding DC power consumption - only $240\,\mu W$ are required, but the CBW is limited.

VI. Conclusion

A comparison of the requirements for mmW-MMIC and the properties of the presented papers, which are summarized in Table II, yields to the findings that the PD approaches of papers [13], [18], [19], [23] seem to be the promising solutions.

Paper [23] is particularly of interest due to the highest used center frequency. Due to the open-loop-architecture, it might be interesting implementing a telecommand controlled tuning possibility or even an automatic tuning feature for the EA or the VDL to counter ageing effects and ensure proper performance over a long lifetime of the linearized PA. This is especially important for satellite applications. Regarding satellite application, the robustness against environmental influences of the proposed circuit design has to be considered.

The theoretical FB approach presented in [12] to enhance linearity by means of delay control could be also of interest due to the investigated frequency range and the given option of tracking the RF envelope power in order to control the power supply depending on the required RF ouput power.

In my opinion, a combination of [13], [18], [19], [23] is the circuit solution for future mmW-MMIC linearization.

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