

University of Stuttgart

Institute of Robust Power
Semiconductor Systems

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Study duration:

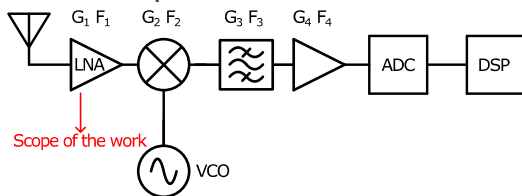
- ✓ Master's Thesis: 6 months
- ✓ Research Project: 3 or 6 months (6 recommended)

Research Project /
Master's Thesis

RF

Design of a Power-Efficient Wideband Low- Noise Amplifier for W-Band Applications in SiGe HBT Technology

Motivation: The W-band (75–110 GHz) is increasingly adopted in high-resolution radar and satellite communication systems due to its short wavelength and compact hardware potential. With congestion in lower bands (e.g., X- and Ku-bands) and growing demand for high-throughput links, interest has shifted to higher frequencies like the V- and W-bands, enabled by advancements in transistor technologies (higher f_T/f_{MAX} , gain, and noise performance). However, W-band signals suffer from significant path loss and atmospheric absorption, degrading signal-to-noise ratio (SNR). To ensure reliable data transmission, preserving SNR through front-end amplification is critical. As described by the Friis formula, the noise figure and gain of the first receiver stage heavily influence overall system noise. Hence, low-noise amplifiers (LNAs), placed after the antenna, are essential. They must offer minimal noise figure, high gain, and linear operation across a wide dynamic range to accommodate variable signal strengths, while maintaining the power efficient operation.



$$F_{overall} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \times G_2} + \frac{F_4 - 1}{G_1 \times G_2 \times G_3} + \dots + \frac{F_N - 1}{G_1 \times G_2 \times \dots \times G_{N-1}}$$

Goals: The objective is to design and implement a schematic / layout (for Master's Thesis) of a wideband LNA covering the entire W-band. The LNA should demonstrate a competitive figure-of-merit (FOM) by achieving low noise figure, high gain, wide bandwidth, high third-order input intercept point (IIP3), and low power consumption, in comparison with state-of-the-art solutions.

Tasks:

- Conduct a comprehensive literature review on wideband LNA architectures, with emphasis on recent topologies and noise reduction techniques.
- Design and verification of the LNA circuit using ADS or Cadence, as if intended for chip fabrication.
- Scientific report and presentation of the work with state-of-the-art comparison.

