

# University of Stuttgart

Institute of Robust Power  
Semiconductor Systems

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Research Work\*  
Bachelor's Thesis\*  
Master's Thesis\*

to be assigned

ILH  
RF-group

## Fast analog loop filter stacked with digitally implemented tracking for a wideband PLL

### Motivation:

Analog carrier recovery for receiver synchronization on the carrier-signal allows extremely high data rates at high carrier frequencies. The analog approach compared to digital synchronization draws less energy as data can be digitized directly in baseband.

For a existing wideband Phase Locked Loop (PLL) (Fig.1) as part of a carrier recovery, an external, controllable loop filter (LF) (Fig. 2) must be designed.

It's application will be in a satellite-groundstation of the [EIVE Project](#), in which it locks on the carrier of an E-band (ca. 75GHz) QPSK-modulated, wideband data signal. The application only allows fast analog loop filter in the direct path, because of very small time delay necessary. For accurate tracking of e.g. doppler shift of the moving satellite, temperature shifts etc. an additional, overlaying digitally implemented filter must be developed.

### Goals:

- Development of a controllable LF as a mixed signal system (fast analog signal throughput via OP-Amp, digital implementation (e.g.  $\mu$ -Controller/controllable OP-Amp etc.) of slower tracking capability (integration).
- Evaluation of correlation between filter parameters and locking behavior (lock range, pull in range, stability etc.) of the PLL / carrier recovery.
- Verification of the latter with a functioning prototype of the analog PLL and the LF.

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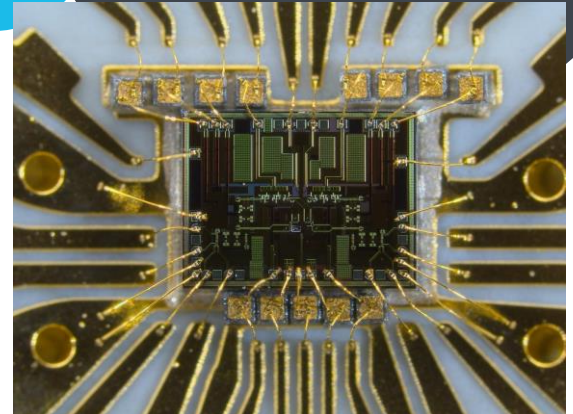


Fig.1 Microscope picture of Costas Loop MMIC (SiGe, 1.5mm x 2mm)

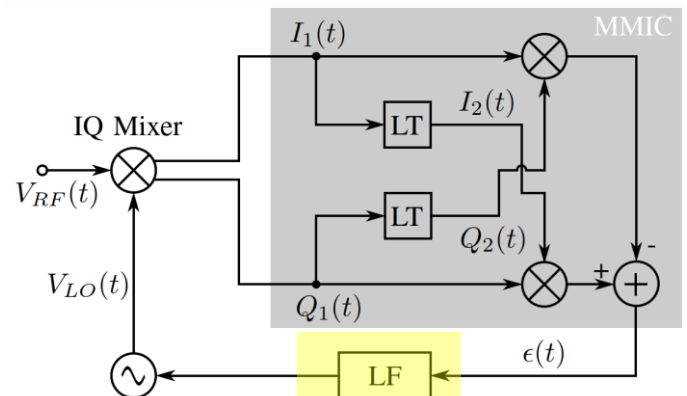


Fig. 2 Scheme of the Costas Loop carrier recovery system

### Tasks:

- Evaluation of required specs for a LF (bandwidth, propagation delay, tracking, controllability etc.)
- Design and simulation of a mixed signal LF
- Design and layout of a prototype PCB
- Design of a rudimentary interface for digital control (e.g. COM port and command line)
- Design of a testbench and debugging of interface

*\*the workload will be adjusted accordingly*

Language: German/English

