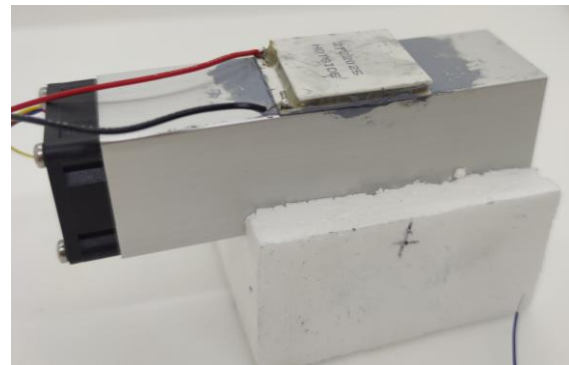


In modern power electronics an ever increase in power density and efficiency is pursued. For thermal modelling and reliability purposes an exact knowledge of the switching and conduction losses is required. Besides a variation of the losses of Wide Bandgap in dependence of parameters like gate-source, drain-source voltage and current, the losses can be prone to aging. Goal of this thesis is to implement a degradation model for a specified Transistor. For this a classic accelerated lifetime-testing approach utilizing thermal cycling with DC- current and a peltier for fast cooling purposes should be implemented. Within the accelerated lifetime test characterization measurements of several parameters should be conducted.



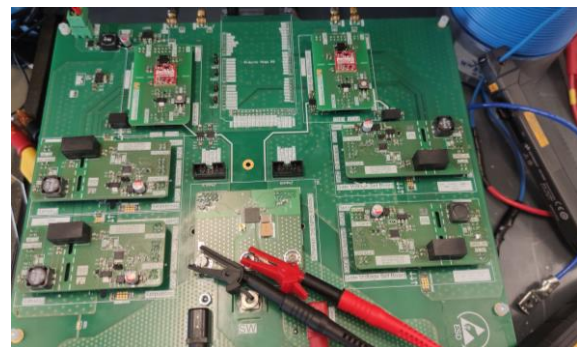
Peltier-Element for accelerated lifetime tests.

Timeplan:

- Familiarization & literature research (10%)
- Construction of accelerated lifetime- test setup (20%)
- Characterization of the degradation measurement in dependence of different parameters (30%)
- Implementation of the degradation model in a simulative approach (25%)
- Thesis writing and presentation (15%)

Helpful previous knowledge:

- Power electronics I / RPSS 1 & RPSS 2
- Matlab/Microcontroller/SCPI programming



Characterization-Board for parameter extraction