Description:

This thesis work involves making a study of available FPGAs suitable for the design of low pass filter with configurable gain and bandwidth. This filter is used as loop filter for carrier and phase synchronizing structures in mmW receivers which are similar to phase locked loops. Further information is can be discussed when interested.

Responsibilities:

- Literature survey on different FPGA and analyse if they are suitable for application or not. If not find alternatives.
- Study of useful algorithms for filter implementations.
- Using suitable coding to implement the algorithm like Verilog, VHDL etc.
- Experimental Validation.
- Prior knowledge of HDL languages is important.

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