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Overview and Evaluation of Current Measurement Technologies for Switching Characterization of GaN Transistors

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***Abstract*—For the characterization of fast switching Gallium Nitride transistors, current sensors with particularly wide bandwidth and low parasitic impedance are required. In this paper, the following sensor types are discussed: shunt, senseFET, current transformer, Rogowski coil, embedded single-turn coil, Hall effect sensor, magnetoresistive as well as giant magnetoimpedance current sensors. Furthermore, the HOKA principle and the active current transformer are presented as hybrid approaches. Different measurement applications call for distinct requirements such as galvanic isolation or integrability, which are met best by different sensor types.**

***Index Terms*—Gallium Nitride, Current Measurement, Current Sensor, Current Sensor Integration, Switching Characterization**

I. Introduction

Transistors based on Gallium Nitride (GaN) are advantageous for power electronic applications with high performance demands due to the wide bandgap of the semiconductor material. It provides a higher breakdown field and better electron mobility than silicon, thus GaN transistors offer higher blocking voltages, a lower on-resistance and enable higher switching frequencies [1], [2].

These characteristics reduce switching losses [1], [3], but regarding the fast switching transients, precise current measurement becomes more challenging, though crucial for effective diagnostics and control applications [2], [4].

Regarding high frequency applications and feedback control, the current measurement is more challenging because the sensors need to be particularly accurate and thus require wide bandwidth [4]. However, current sensors introduce additional parasitic impedances into the device circuit which alter the switching transients [1]. The impact of these parasitic effects is particularly strong for fast switching transistors [1], [2], [5].

The aim of this paper is to give an overview of common and emerging current measurement technologies suitable for the switching characterization of GaN transistors. The paper is organized as follows. In section II, several measurement approaches are described. Section III presents different requirements which should be fulfilled by a current sensing method. These requirements are taken into account when the respective approaches are compared and evaluated in section IV. Section V concludes the paper.

II. Overview of current measurement

In the following subsections, different current measurement concepts are presented. They are categorized into three groups: Sensors based on voltage drop measurement (II-A, II-B), sensors utilizing electromagnetic induction (II-C, II-D, II-E) and sensors which are sensitive to the magnetic field created by the current to be determined (II-F, II-G and II-H). Subsequently, hybrid approaches are presented in II-I.

A. Shunt

Shunts are directly introduced into the path of the current which is determined by measuring the voltage drop along the shunt [5], [7]. The resistance value is a trade-off between low losses and oscillation damping effect, but always in the range of small values up to hundreds of milliohms [8].

Simple shunts are not well suited for high frequency applications, because their resistance is altered due to skin and proximity effect [5], [9]. There are two alternative designs:

Coaxial shunts minimize frequency dependency, consisting of two tubes carrying current in opposite directions in order to cancel out the magnetic field inside the inner tube [7], [9]. The downside of commercially available coaxial designs is their large package size and consequently the additionally introduced inductance causing response delay [5], [8]. With the miniaturized shunt design depicted in Fig. 1, this inductance is reduced resulting in a very accurate output signal [6].

Another option for minimizing parasitic effects is using thin film SMD shunts. They offer a particularly low package inductance due to the small size [8], [10] and are very suitable for full integration into the device manufacturing process [11].

As a consequence of the measurement principle, shunts lack galvanic isolation and decrease the device efficiency due to the

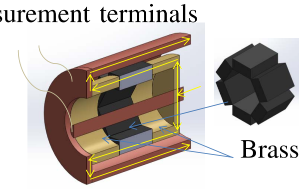


Fig. 1: Miniaturized coaxial shunt from [6]

inserted ohmic resistance [9]. Moreover, the resistance values of shunts exhibit temperature dependency [4]. Benefits are the wide bandwidth from DC up to GHz range, no saturation limitation and low production cost [3], [8], [9].

B. SenseFET

The most simple method to determine the drain-source current flowing through a MOSFET is to measure the drain-source voltage drop, but due to the very low on-resistances of modern MOSFETs, it is challenging to filter and amplify the low measured voltages [12].

A common integrated measurement method is the so-called senseFET technique [2], [13]–[15]. In a power module with many transistors connected in parallel which have the same gate-source signals, one of them serves for measuring purposes with its source pin connected to a series sensing resistor. The current flowing through it represents the main current flow and is determined by measuring the voltage drop along the sensing resistor.

In [4], a similar technique called SenseGaN is evolved. Challenges are the impacts of current ratio mismatching and temperature dependency of the sensing resistor and the dynamic on-resistance of the transistors. These are minimized by virtual grounding and low sensing resistance values.

C. Current transformer

In a current transformer (CT), the to be measured AC current flows through the primary side of a transformer, which creates a magnetic field concentrated by the core, inducing a proportional current on the secondary side.

Especially the bandwidth of a CT is the most crucial parameter for the switching characterization of fast waveforms. If the design provides a low stray capacitance and low leakage inductance as well as high magnetizing inductance, a bandwidth up to approximately 20 MHz is achieved [17]. But due to the additional loops in the main current path, parasitic inductance is introduced in the device circuit [8], [9]. Furthermore, the magnetic core exhibits saturation leading to current limitation and affecting the accuracy [9].

The mostly bulky size of CTs limits the integration capability [8], [9]. Regarding this, two approaches are being pursued. First, Reference [16] presents a core-less PCB-based CT with a U-shaped primary side which is depicted in Fig. 2. Secondly, [18] and [19] propose a CT with a core composed of silicon steel laminations which is adjustable to the respective current path in order to minimize stray inductance.

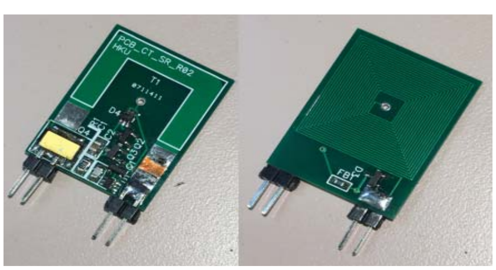


Fig. 2: Planar PCB-based CT from [16]

D. Rogowski coil

Rogowski coils are based on the principle of electromagnetic induction. It consists of a coil wound around a toroidal non-magnetic core through which the current-carrying conductor is led [9], [20]. In the coil, a voltage proportional to the derivative of the current is induced [9], [20]. An integrator is needed to provide a value proportional to the current [9], [21].

It is very suitable for the measurement of fast switching transients, providing a theoretically very high bandwidth, galvanic isolation, low cost, no saturation due to the air core and a wide range of current values [3], [9], [20].

The achieved bandwidth is dependent on the number of windings. These are the outcome of a trade-off between minimized sensitivity to external magnetic fields and low parasitic capacitance [5], [10]. Two Rogowski coils with different bandwidths could be combined, but the time constants of their integrators must be accurately matched [22]. The accuracy is also dependent on the sensor position and orientation [18].

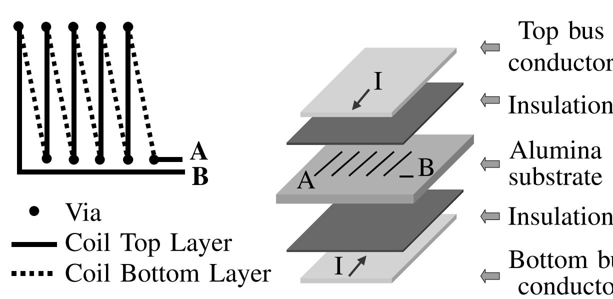
Furthermore, the induced voltage is affected by capacitive coupling effects due to high voltage gradients in the device. This can be overcome by shielding, but this reduces the bandwidth [23]. Another solution is a differential measurement with two Rogowski coils leading to the cancellation of the capacitive voltage drop [23], [24].

Planar PCB-based Rogowski coils as illustrated in Fig. 3 are developed in order to achieve full integration [9], [21], [24].

Though, as Rogowski coils provide no DC measurement, they are often combined with other sensors, see section II-I.

E. Embedded single-turn coil

With an embedded single-turn coil (ESTC) inside the PCB of a device along the power loop, the current is determined by making use of the parasitic inductance in the circuit [5]. This principle is based on magnetic coupling, hence a voltage across the sensing coil proportional to the derivative of the drain current can be measured. The distance between the two loops is minimized in order to increase the coupling, whereas the introduced parasitic inductance is small because the pick-up coil has only one winding. But due to the measurement



(a) Top view

(b) Exploded view

Fig. 3: PCB-based Rogowski coil from [9]

principle, DC currents cannot be detected. This principle was presented just recently, therefore not all characteristics are reported in detail yet.

F. Hall effect current sensor

The Hall effect describes the occurrence of a voltage across a current-carrying conductor which is placed in an external magnetic field. Hereby, the directions of the voltage, current and magnetic field are oriented perpendicular to each other [25]. In the context of a Hall effect based current sensor, the external magnetic field is created by the current which is to be measured [26], [27]. The sensor consists of a ferromagnetic ring with a small air gap placed around the examined conductor focusing the magnetic field [26]. In the air gap, the sensor contains a thin strip of metal along which a current is applied. Due to the Hall effect, a voltage proportional to the current to be determined is measured across the metal strip.

This sensor provides galvanic isolation and DC current measurement. Though, it is bulky, has limited bandwidth up to 1 MHz and limited peak current due to core saturation. It exhibits temperature dependency as well as a significant insertion impedance and the accuracy depends on the core position [3], [9], [25], [26], [28].

Core-less Hall effect sensors provide a smaller size and low cost. But their accuracy is highly dependent on the position and they lack sensitivity because the magnetic field is not focused by a core [27]. This is improved by using a U-shaped conductor with the sensor placed inside the U [27] and a complementary configuration which removes possible off-set voltages as well as position dependency [26], [29].

G. Magnetoresistive current sensor

The two most prominently used magnetoresistive (MR) sensor types are anisotropic magnetoresistors (AMR) and giant magnetoresistors (GMR). Both types consist of alternating layers of ferromagnetic and non-magnetic material which exhibit a change of their resistances dependent on an external magnetic field [9], [30]–[33]. Across all layers, a sensing current is applied in order to determine the resistance of the stack. The sensors are usually arranged in a Wheatstone Bridge which eliminates offset, influence of interfering magnetic fields and temperature drift [30], [31], [33]–[35]. The resistance change is not completely linear which results in a limited current range to avoid hysteresis [32].

GMR sensors offer higher bandwidth and sensitivity than AMR sensors, thus have faster transient response [30], [33]. Sensitivity at high frequencies is further increased with the help of magnetic field concentrators which are put on top of the PCB trace minimizing magnetic field distribution caused by skin effect [30], [36].

MR sensors provide a non-invasive measurement with galvanic isolation, very low losses and a bandwidth in the single- and double-digit MHz range [9], [30], [31], [35], [36]. But the production technologies including molecular beam epitaxial growth and electron beam evaporation are complicated and difficult to integrate in the transistor manufacturing process [9].

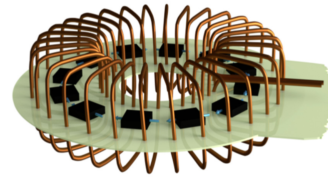


Fig. 4: HOKA with MR sensors and Rogowski coil from [42]

H. Giant magnetoimpedance current sensor

The giant magnetoimpedance (GMI) effect occurs in soft magnetic amorphous wires and ribbons carrying an RF current whose impedance changes dependent on an external magnetic field [9], [37]–[39]. Analogous to a MR sensor, a particular current is determined by placing the GMI sensor in the created magnetic field of the current. GMI sensors offer high sensitivity, wide bandwidth and enable miniaturization [9], [40]. They are even more sensitive than the GMR sensor [9].

Though, their high sensitivity to external magnetic fields, temperature dependency and non-linear behavior are challenges to be faced [9], [41]. Temperature dependency can be suppressed by differential measurement with double-core structure [37], [38], [41]. Bias coils [38], [41] or a permanent magnetic core providing a bias field [37] are used in order to achieve an operating point in the linear part of the MI characteristics. Furthermore, the cores must not be stressed mechanically because the GMI effect is highly dependent on deformation [38]. GMI sensors are not fully developed for commercial use due to their complicated structure and expensive design demands for accuracy [4], [41].

I. Hybrid approaches

a) HOKA: For this principle, the low frequency range sensor, e.g. Hall or MR sensor, must have an output proportional to the sensed current with a low-pass transfer function and the output of the other sensor, i.g. Rogowski coil, must be proportional to the derivative of the current. Both signals are multiplied with scaling factors, then added and sent through a low-pass filter which lets pass the low frequency share and works as an integrator above the cutoff frequency [42], [43].

This principle is advantageous due to the increased and flat band bandwidth from DC up to double-digit MHz range. Moreover, no additional integrator is required for the Rogowski output [42]–[45]. In [45], a coaxial setup is presented in order to achieve very low additional impedance. The design proposed in [42] is shown in Fig. 4.

b) Active current transformer (ACT): An ACT combines a CT measuring currents with high frequencies and a Hall effect sensor for low frequency signals [5], [46], [47]. But just like the two underlying concepts, it is limited by saturation and frequency dependency of the core and by the amplifier bandwidth [5], [47]. Nevertheless, ACTs provide a measurement range from DC up to double-digit MHz and low cost [46], [47].

TABLE I: Comparison of current sensors

		Bandwidth	*Parasitics*	*Sensitivity*	*Hysteresis*	*Galvanic isolation*	*Noise immunity*	*Temperature drift*	*Size*	*Integrability*	*Cost*
Shunt	coaxial	DC..5 GHz	low	high	no	no	very good	yes	small	good	low
	SMD		very low				good		very small	excellent	
SenseFET		DC..N/A	low	high	no	no	good	yes	small	excellent	low
CT		5 kHz..20 MHz	high	medium	yes	yes	good	no	medium	possible	medium
Rogowski		100 kHz..100 MHz	medium	high	no	yes	medium	no	medium	possible	low
ESTC		N/A	low	N/A	no	yes	N/A	no	small	good	low
Hall		DC..1 MHz	medium	medium	yes	yes	medium	yes	medium	possible	medium
MR	AMR	DC..2 MHz	low	high	yes	yes	good	yes	very small	complicated	medium
	GMR	DC..5 MHz		very high							
GMI		DC..30 MHz	low	very high	yes	yes	good	yes	very small	complicated	high
HOKA	MR	DC..100 MHz	medium	high	yes	yes	medium	yes	small	complicated	medium
	Hall								medium	possible	medium
ACT		DC..50 MHz	high	medium	yes	yes	good	yes	medium	possible	medium

III. Measurement requirements for switching characterization

Multiple requirements determine the choice of the sensing method.

A. Requirements arising from GaN transistor characteristics

GaN transistors enable very fast current switching transients in the range of single-digit A/ns. Therefore, a bandwidth of at least several tens of MHz is necessary for precise measurement [8], [21], [42], [48]. Furthermore, parasitic inductances make a great impact on the switching behavior, resulting in oscillations, ringing and voltage as well as current spikes, leading to increased switching losses [1]–[3], [5]. Consequently, two requirements are noted:

- Wide bandwidth (tens of MHz up to GHz range)
- Low additional parasitic inductance and resistance

B. Requirements arising from high performance demands

For safe and accurate measurement, crucial factors are:

- High sensitivity
- No current limit due to saturation/hysteresis
- Galvanic isolation
- Noise immunity
- Temperature stability

C. Requirements arising from sensor integration

Full integration of current sensors into integrated power electronic modules (IPEMs) minimizes cost, dimensions and interferences [9], [25]. In this regard, demands are:

- Small sensor size
- Compatibility with the IPEM manufacturing process
- Low cost

Size and compatibility are decisive upon the possible integration levels. Furthermore, a small sensor size helps achieving a small parasitic inductance which is often caused by the larger trace on the PCB board and package inductances, not necessarily by the sensor itself [1], [8].

IV. Comparison of the current sensors

In table I, all presented sensor types are compared regarding the requirements listed in section III. The vertical lines group the different sensor type categories, the horizontal lines indicate the different requirement groups.

The sensors of the first group, shunt and senseFET, do not provide galvanic isolation. However, shunts offer the widest bandwidth along with easy integrability making them a prime candidate for applications with low common-mode voltage.

Rogowski coils exhibit the second highest bandwidth, but do not enable DC measurement, which is why a HOKA combination with an MR sensor is a more favorable option.

Ferromagnetic cores increase the device costs and sensors comprising a core are unsuitable for full integration into an IPEM due to their dimensions, thus core-less PCB-based Hall sensors, Rogowski coils and current transformers are designed. These approaches are successful, yet exhibit lower sensitivity due to the non-concentrated magnetic field.

For sensors which exhibit temperature drift, thermal considerations at design level and temperature capture are necessary for accurate signal processing. Devices with hysteresis require a current limit in order to operate in a linear range.

GMI sensors are promising in terms of bandwidth and sensitivity, but their design and manufacturing process is complicated which makes integration difficult.

V. Conclusion

In this paper, common and emerging current sensor types as well as hybrid concepts are presented. Requirements for sensors suitable for switching characterization of fast GaN transistors are discussed, regarding transistor characteristics, sensor performance demands and sensor integration. Because no sensor type can meet all requirements, the specific application decides on the most important demands and consequently on the suitable sensor. For applications with low common-mode voltage, shunts are the best choice due to the particularly wide bandwidth. A HOKA sensor based on a Rogowski coil and MR sensors is a good option for higher voltages.

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Advanced cooling technologies for power electronic devices

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Abstract: With rising energy consumption in mobile electronic devices, fast and powerful charging methods are becoming increasingly important. One of the most limiting factors for power conversation in charging circuits is heat dissipation. This paper reviews the state of the art of latest technologies for heat distribution and examines their practicability for cooling power electronics in consumer devices. Basic concepts of heat spreading via carbon graphite, heat pipes, vapor chambers, Peltier-elements, Piezo- and EHD-fans are described. Their advantages and disadvantages in properties like costs, thermal conductivity, flexibility and commercial availability are shown. Based on these considerations, the use of these concepts in an exemplary 200 W power supply for consumer appliances is discussed.

Keywords: cooling, heat spreading, heat pipe, vapor chamber, carbon graphite sheets, EHD-cooling, Piezo-fan

I. Introduction

To increase power densities in charging adapters, either the efficiency of power electronics (PE) or the heat extraction of dissipated energy must improve. While the efficiency of a power conversating circuit is limited by the driver and the PE itself, the heat extraction is limited by the thermal conductivity from the PE-hotspots inside the device to the surrounding ambient.

The thermal conductivity of the whole device depends partly on the packaging of PE components and the heatsink, but also hugely on the interface materials between hotspots and heatsink. The entire thermal resistance can be modelled by adding all thermal resistances of each material, as shown in [1].

In most consumer electronics (smartphones, laptops, power supplies) the casing acts as a heatsink. As it is the goal to minimize the size of a power supply, the area and thereby the properties as a heatsink are mostly predefined. This also applies to the packaging of PE components and their thermal behavior, since consumer devices should be built out of on-the-shelve products, which are specified by the manufacturer.

Consequently, this paper focusses on technologies, which improve the thermal conductivity inside the device beginning from transistor junctions to the heatsink interface.

Papers like [1] and [2] are already giving a wide-ranging overview on many different technologies, without going into too much detail. Therefore, the goal of this paper is to prioritize the most promising technologies and discuss them more detailed, with the focus on applying them in consumer electronics.

II. Passive Technologies

Passive Technologies enhance heat flow, without the use of extra power.

A. Carbon graphite sheets

To ensure a good heat flux, materials with a low thermal resistance, like aluminum and copper are widely used for conducting heat to low temperature areas, e.g. along a printed circuit board (PCB). Lately thermal management products out of graphite have entered the market, which has a maximum lateral thermal conductivity of 1950 W/(m*K). That is up to 5 times higher compared to copper [3].

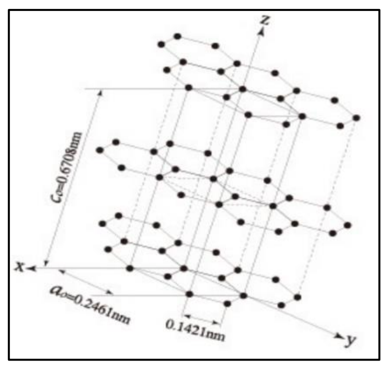

Figure 1: Graphite crystal structure, source: [4]

Graphite consists of multiple layers of two-dimensional carbon crystal structures (see Figure 1). It is called *Graphene* if it consists out of just a single layer. Due to this structure, the vertical thermal conductivity (through the crystal layers) is very low, just around 5 W/(m*K), which makes the orientation of the layers significant [5].

There are several ideas to improve thermal conductivity with the new material. Papers [6] and [7] propose to build a layer inside a PCB out of graphite sheets or a graphite-copper composite material to distribute the heat homogenous over the whole area.

A few graphite sheets are already commercially available. References [4] and [8] are graphite foils made from natural graphite and their structure is amorphous. This is the reason why their thermal conductivity is relatively poor (200 W/(m*K)) compared to Panasonic's pyrolytic graphite sheets with 1950 W/(m*K) [3]. Pyrolytic sheets are made with a chemical-vapor-deposition-process and thermal annealing. This results in a highly orientated crystal structure [5].

Besides graphite sheets for lateral heat spreading, there is also a concept for vertical conductivity, where the crystal layers are vertically orientated [9]. This could be useful for thermal interface materials (TIMs) when PE-devices are directly attached to heatsinks.

Another already available product is Panasonic's Graphite-Pad [10], which has a foamlike structure for three-dimensional heat spreading. But due to the amorphous structure, the thermal conductivity is just 13 W/(m*K).

Another advantage of graphite sheets and foam is their flexibility, which makes them bendable and compressible. This is useful as shown in [11], where a graphite sheet was fitted inside a casing to spread the heat homogenous along it.

In terms of costs, graphite sheets are less expensive than Panasonics Graphite-Pads [12] [13], but costs of all graphite products hugely depend on their size. Due to the flexible properties of graphite products it should be possible to use on-the-shelve products for many different applications, which could drop the prices in the future, because of large manufacturing quantities.

B. *Heat pipes and vapor chambers*

Heat pipes (HP) and vapor chambers (VC) transport heat by vaporizing fluids at hotspots and letting them condense at colder areas. While heat pipes establish a heat flow in just one direction [7], vapor chambers distribute the heat two-dimensional in a plane. The thermal conductivity of HPs and VCs lies between 10 kW/(m*K) [14] and 50 kW/(m*K) [15], which is 5 to 25 times higher than graphite sheets.

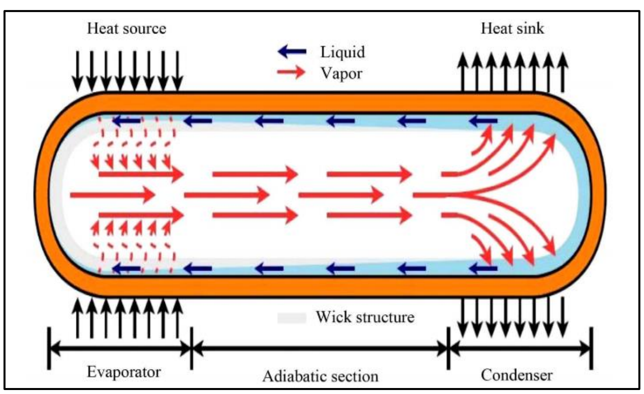

Figure 2: Heat pipe and vapor chamber principle [16]

Figure 2 shows the concept of a wick-based HP. Wick structures along the side of the HP provide capillary forces, which, after condensation, carry the liquid back to the evaporator [17]. Another concept for HPs are oscillating HPs (OHPs), which work by establishing a circular flow of the liquid, caused by pressure differences between hot and cold sides. OHPs are more flexible in terms of geometry and easier to produce, because the wick is not mandatory [15].

The functionality of HPs and VCs depends on many parameters like for example:

- Volume, shell-material, diameter.
- Wick density and structure.
- Chemical characteristics of working fluids and filling level [18].

Therefore HP- or VC-Systems are hard to optimize and have many failure options, which might be caused by variety of possible errors in production.

Another concern for functionality is gravity, which can lead to problems when the capillary forces are too weak, or the viscosity of the filling fluid is too high. [18] [19]

Another problem is that HPs and VCs are mostly made of solid aluminum or copper, materials that lack flexibility, which can make it difficult to use on-the-shelve-products for compact devices. This can raise prices if there is a need for custom-built shapes in applications with small quantities. Nevertheless, for large quantities it must be considered that costs for copper and aluminum are lower than for graphite or active cooling technologies.

There are ideas to improve heat flux in devices by embedding HPs in PCBs [7] [20], heatsinks and casings [21]. It is also proposed to embed VCs in silicon chips like in [22] [23] [24] shown. In all experiments with these concepts heat conductivity was improved, but also challenges in manufacturing, e.g. inserting a right amount of working fluid into HPs, were documented.

III. ACTIVE TECHNOLOGIES

Active technologies improve the thermal conductivity by using additional power. These technologies are more expensive than the previous discussed but can be used in combination with them to increase heat flow further.

A. *Peltier-Elements (Thermo-electric-couples)*

In a Peltier-Element, heat is transferred inside a material by applying a bias current, like shown in Figure 3. This is used in [25] for cooling a LED and transferring dissipated heat to a heatsink.

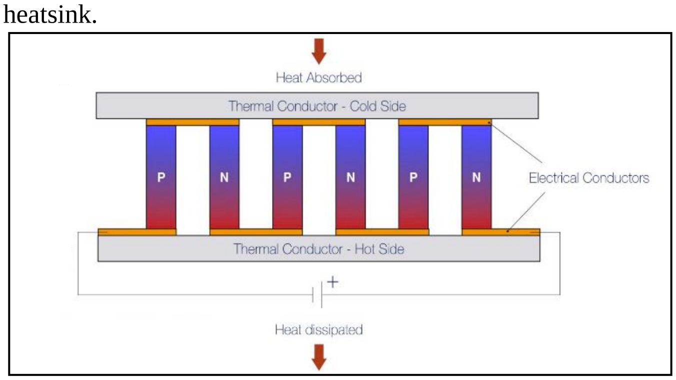

Figure 3: Principle Peltier-element [26]

The cooling results are satisfying and could help to extend the lifetime of the electronic components. Additionally, active cooling can lower the electrical resistance of transistors, which can save some dissipated power [27]. Unfortunately, it is inefficient because the Peltier-element itself consumes a lot of power. As a result, the heatsink gets hotter than in the setup without the Peltier-element, which makes it unsuitable for devices where the heatsink is limited, e.g. in consumer electronics.

B. Piezo-fans

Piezo-fans can be used for moving air or fluids. They work by applying an AC-voltage on a piezo crystal, which creates a mechanical oscillation. This oscillation is transmitted to a small plate for generating ventilation. This concept is displayed in Figure 4 (left).

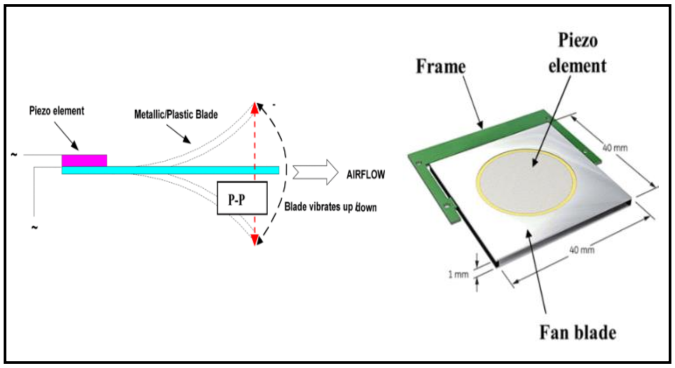

Figure 5: Piezo-fans, sources: left [28]; right [29]

In comparison to normal fans, Piezo-fans need less power and produce less noise [28]. Furthermore, they are way more compact. In [30] and [29], piezo-fans are used to dissipate power in the range of 5 W to 10 W to ambient Air with a height of the fan of just 3mm.

Miniaturized piezo-fans like shown in Figure 4 (right) are hardly commercially available yet, which makes it difficult to predict prices.

C. Corona wind generators and electrohydrodynamical (EHD) fluid pumps

Corona wind fans generate an air flow by ionizing air molecules, which then get attracted by an opposite charged electrode (see Figure 5). These fans require high voltages but could be used for improving cooling via forced convection. EHD-pumps move fluids with the use of the same principle [32].

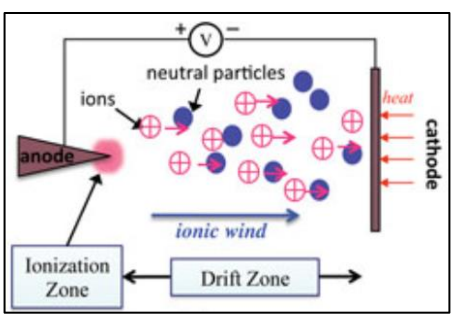

Figure 4: Principle for EHD wind generation [31]

Although EHD based cooling is currently in research state, it is estimated that EHD cooling devices will have a small power requirement [33] [34]. Other advantages are that they have no moving parts and produce less noise compared to conventional fans. In addition, their size and form are flexible, and it is expected that they are easy to miniaturize and could be embedded into chips [35].

EHD based air blowers were used in [34] to cool a laptop. The modified laptop has shown the same behavior as the ordinary version with a fan and did not interfere with sensitive components like WIFI, the touchpad or the display.

EHD fluid pumps are expected to be useful in heat pipe systems to improve the fluid flow and prevent failure mechanisms caused by gravity [33].

There currently is just one company which manufactures and distributes EHD driven fans [36], but there is no information regarding their costs or test reviews available yet.

IV. Practicability for Consumer Devices and Suggestion for Exemplary 200 W Power Supply

The technologies discussed in the previous sections are hard to compare in numbers because crucial properties like e.g. thermal conductivity and costs hugely depend on the geometry, thermal interface structures of the applied device and manufacturing quantities.

In [1] a comparison between many technologies was approached. But due to the huge differences between the technologies and different fields of usage, the comparison is very qualitative, and it seems partly arbitrary.

Hence, the following suggestions for implementation in an exemplary device are based on the previously described advantages and disadvantages.

The exemplary 200W power supply should have dimensions of roughly 10 cm * 4 cm * 4 cm. Previous experiments by [37] have shown that the casing as a heatsink can dissipate about 5 W of power to the ambient, when the heat is distributed homogenously on the surface. This results in a required efficiency of 97,5% for the PE-circuit.

For small manufacturing quantities, graphite sheets and pads should be considered due to their flexibility and possible usage of on-the-shelve products. The graphite sheets could be fitted around the inner surface of the casing and could directly be attached to the PE-components. Also, graphite pads (foam) could be tested, since their thermal conductivity is three-dimensional. Graphite technologies are estimated to have the best reliability, since they have less possible errors than others.

For large manufacturing quantities, custom build copper HPs are expected to be less expensive and have a better thermal conductivity. It should be researched if OHPs could get embedded into the synthetic casing of the power supply and get attached to a HP-system on the PCB, surrounding hotspots. An OHP system should be preferred to a wick-based system due to manufacturing difficulties.

Peltier-elements are less useful in this use case because of their high use of extra power, which also must be dissipated at the heatsink.

If costs are a less important aspect and the focus is on best possible thermal conductivity, active technologies like piezo- and EHD-fans should be considered for cooling the device via forced convection. But due to few commercially available components, the practicability and reliability for big manufacturing quantities is difficult to estimate. Future research and market observation will provide clarification.

V. Conclusion

This paper develops an overview of the most promising cooling technologies for consumer PE devices. Advantages and disadvantages are phrased and suggestions for cooling an exemplary power supply are made. Future experiments, research and market observations will show which technologies are most suitable for a wide variety of appliances.

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Radiation Hardness of SiC MOSFETs

An overview of radiation damage mechanisms in SiC MOSFETs

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***Abstract*—With this paper the author tries to give an overview of failure mechanisms in Silicon Carbide MOSFETs caused by cosmic radiation. Cosmic radiation is a big factor in power electronics reliability in terrestrial and even more so in aerospace applications. This paper will look at Total Dose and Single Event failure mechanisms caused by various types of radiation commonly found in terrestrial and primary cosmic radiation with a focus on radiation hardness of commercially available high voltage power Silicon Carbide MOSFETs.**

***Index Terms*—Silicon Carbide, radiation hardness, cosmic radiation, failures mechanisms, MOSFETs**

I. Introduction

As reliability of power electronics is one of the major engineering concerns it is important to understand that cosmic radiation is one big contributor to premature failures if not properly addressed in the design and component choices. Since the commercial availability of silicon carbide devices many studies have shown silicon carbide (SiC) to have superior radiation hardness in comparison to silicon devices. [1]–[8]

This is partly because silicon carbide is a wide band gap semiconductor (3.25 eV for 4H-SiC) with better thermal conductivity ($3.7\frac{W}{cm\cdot s}$), low intrinsic carrier concentration ($5\cdot10^{-9}$ cm^{-3} @ 25°C), stronger covalent bonding between the Si-C in silicon carbide as compared to Si-Si in silicon, higher critical electric field strength($2.2\frac{MW}{cm}$), higher displacement energy (20–35 eV) and it requires energies of 8-9 eV to produce an electron hole pair which is three times higher than in silicon. [8]

All this makes silicon carbide a promising candidate for the future of power electronics with higher power density, reduced weight and high reliability. Not only for terrestrial, but also for aerospace applications.

But as cosmic radiation consists of various kinds of radiation it is important to understand the failure mechanisms caused by them. The primary cosmic radiation (Primary CR) consists of high energy photons, protons, heavy ions and electrons. This high energy particle radiation does not penetrate our atmosphere. The terrestrial cosmic radiation (Terrestrial CR) is caused mainly by spallation reactions between the high-energy primary cosmic radiation and the upper atmosphere. This causes neutron showers in our atmosphere that reach all the way down to the sea level, and make up the primary part of the terrestrial cosmic radiation. In Fig. 1 the Terrestrial CR flux is shown in dependence of the altitude, with a peak in flux at just above 15 km.

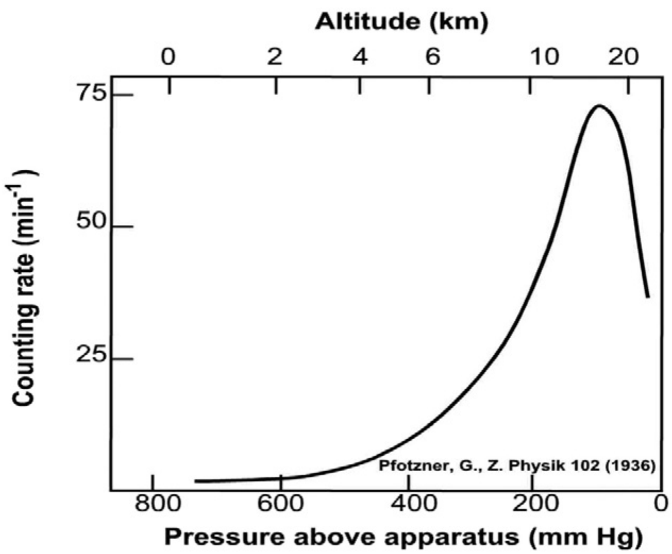

Fig. 1. Cosmic ray intensity (mainly terrestrial neutrons) versus altitude (G. Pfotzner 1936) [9]

II. Total Dose Effects

In this section we look at the electrical parameters shift due to radiation exposure. This changes the device properties until they are not in the design range anymore and causes device failure or deterioration because of the total absorbed dose. For different kinds of radiation there are different mechanisms that cause the devices properties to change.

A. Ionizing radiation

As high energy photons are almost only able to free charges the effect is very minimal in regions that are conducting, generated electron-hole pairs recombine within nanoseconds [8]. So that the region of interest for a MOSFET and ionising radiation is the MOS capacitor, as trapped charges in the oxide or interface effects in oxide semiconductor interface severely changes the properties of the device. As for the gate oxide most trapped chargers are positive, primarily holes trapped in oxygen vacancies [4]. Tests have shown that the SiO_2 gate oxide in SiC MOS structures has less than 5% hole trapping, which is excellent for non hardened power devices. Different to Si the overall interface state generation is quite low compared to oxide charge trapping [4], [10]. Also it seem that no interface dangling bond defects are generated, but substantial changes in interface structure are measured, which seem to have no significant effect on the device operation [4]. Even at 6 Mrad (Co60 γ-ray) the interface trap density only increased 9,7% [4]. Tests on 1200V SiC MOSFETs have shown only small changes in threshold voltage ΔV_{TH}, e.g. ΔV_{TH}=-1 V @ 400 krad [1] or ΔV_{TH}=-1.5 V @ 300 krad [2] (both Co60 γ-ray source @ 25°C). Only at higher doses the V_{TH} shift renders the device inoperable. At even higher irradiation levels the gate drain capacity C_{GD} starts to rise significantly [2]. As it is clearly the gate oxide that defines the ionizing radiation robustness, it can further be increased by e.g. the use of non nitrated SiO_2 (which also traps negative charges which partially compensate the trapped positive charge [10]) or other more radiation hard dielectrics like Al_2O_3 [8]. These tests also showed no increase in leakage, as found in silicon devices, and no gate oxide damage.

B. Electron radiation

The primary effect of electron radiation is not different from ionizing radiation. As it causes direct charge transfer and secondary electron-hole pairs, which also generate trapped charges in the oxide and interface which in turn leads to lowering of V_{TH} until the device is inoperable. But as electrons also have mass they are able to knock atoms out of the lattice. Under certain circumstances irradiation of the device with electron radiation can improve device parameters before the ionizing effect renders the device unusable. Irradiation with e.g. 15 MeV electron radiation has shown to increase channel mobility and decrease bias stress-induced V_{TH} variations [11], in contrast to silicon devices [3].

C. Proton and Neutron radiation

The main cause of device damage is still ionization (95% of the proton energy is lost to electronic interactions [8]), but as protons have more mass they are more likely to knock atoms out of the lattice which deposit charge along their paths. They are more capable to introduce free charge into the device. The displaced atoms cause further defects in all regions, but primarily bulk defects [12]. The protons also cause a very low level of hydrogen implantation. Proton spallation (nuclear reaction) events are more unlikely compared to neutrons, only very high energy protons cause a significant amount of spallation events [9]. But this indirect ionization via spallation, as shown in Fig. 3, deposits the most charge. Lower energy proton irradiation has shown similar effects as electron irradiation, increased channel mobility and lower V_{TH} instability, but as always a total lowering of V_{TH} through ionizing effects. The initial positive effects of the irradiation in [9] is tried to be explained by nitrogen hydrogen diffusion and the formation of a sub-oxide. Simulation for low energy protons have also shown an angle dependency of radiation induced parameter shift [12]. Irradiation tests have also shown that high energy proton sources can be used for accelerated testing if the proton energy is higher that 150 MeV, as the induced damage is very similar to neutron radiation [9].

But as protons may be well shielded in real world applications, high-energy neutrons are the particles of most concern, with regard to reliability. As neutrons are uncharged they are far more penetrating and have a higher probability to knock lattice atoms out (as shown in Fig. 2), with the side effect of the deposition of even more charge by knocked out lattice atoms. With the occurrence of spallation the highest amount of charge is generated (Fig. 3) (for light particle irradiation), only heavy ions can free a similar or even higher amount of charge. The charge generation can be so great that it causes single event failures. Because of this neutron radiation tests are mostly concerned about single event failures. Neutron radiation also degrades the MOS structure by ionization and generates bulk and interface defects by lattice atom displacement. Numerical simulations have shown that the ionization is most influential in the degradation process by introducing interface states and oxide charges. [8]

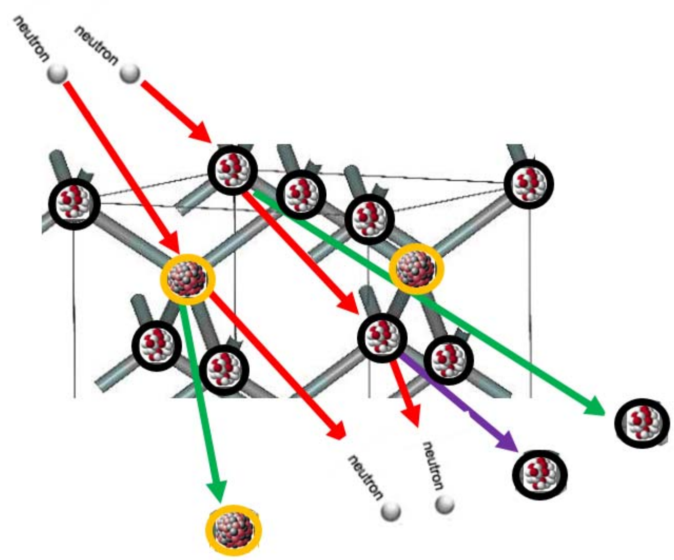

Fig. 2. Neutrons knock lattice atoms off their sites, and the knock-ons deposit charge along their paths in a device [5]

D. Heavy Ion radiation

Except for the direct ionization that can cause single event failures heavy ions cause elastic scattering (displacement damage) at the oxide/SiC interface, as well as in the bulk material [14]. Since SiO_2 seems to be very sensitive to ion induced displacement damage, gate leakage is the dominating failure mechanism [1], [14] for blocking voltages below the single event failure threshold. Tests on 1200V SiC MOSFETs with 15 MeV Xenon ion radiation and blocking voltages below 500V have shown gradual degradation, especially increase in gate and drain leakage, with the gate leakage as the determining factor. No significant V_{TH} change was observed [1].

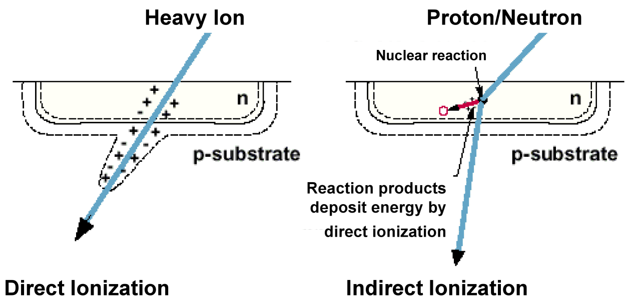

Fig. 3. Direct and indirect ionization [13]

Further tests have shown Al_2O_3 as gate oxide to be less sensitive to ion irradiation displacement damage than SiO_2 [14].

III. Single event failures

Single event failures (SEF) are failures by a single radiation event with enough energy to cause a catastrophic device failure, mostly by a temporary short of the device or gate rupture. Such an event can only be caused by a particle of enough energy, so neutron and ion radiation are the most probable causes. The single event failure rate is measured in FIT/device, which is defined to be one fail in 10^9 device-hours [9].

As reliability requirements for modern power semiconductors (single chip) may range from 0.01 FIT/device to 100 FIT/device, accelerated testing is necessary to reduce the testing time to a sensible amount [9]. For accelerated testing spallation neutron sources and high energy proton sources ($>$ 150 MeV) are used. As neutrons in the energy range of 50-200 MeV deposit the most charge in the device, neutron sources have to be at least in that range to be acceptable for testing [9].

Tests have shown that below a certain voltage, usually around 65 to 70% of the nominal voltage of a device, very few single event failures occur. The failure rate increases exponentially with increasing voltage beyond that point. For applications requiring high reliability the applied voltage is therefore usually limited to approximately 70% of the nominal voltage in silicon devices to achieve low enough failure rates [9].

A. Neutron radiation

The neutron induced single event failure is initiated by energetic secondary particles produced by nuclear reactions (spallation) or collisions of high energy neutrons in the semiconductor device. Depending on the primary neutron energy a multitude of reaction channels exist. Charged spallation fragments will lose their kinetic energy to the electron gas of the solid and thus create a localized and dense plasma of electron–hole pairs within the semiconductor substrate. In the high electric field region of a reverse biased / off-state power device the initial charge deposited by the secondary atoms is amplified through avalanche multiplication [7], which creates a "streamer"-like discharge, much like a gas discharge [9], which also exists in solids. As a consequence the power devices are short-circuited and broken down, which permanently damages the device.

The single event failure probability increases exponentially with the applied voltage above a certain threshold voltage. In Fig. 4 the FIT rates of 1200V devices are shown, one can clearly see that with rising blocking voltage the FIT rate increases, but only after a certain threshold voltage. This indicates a need for a certain field strength in the semiconductor material to cause this kind of single event failure. This threshold voltage is also device and material dependent, as the inclinations of the fitting lines show almost identical inclinations for the same device type or material [7].

Experimental and simulation results suggest a difference in single event failure mechanism between SiC and Si power devices. Energetic secondary carbon atoms are generated by the nuclear reactions and the collisions between the terrestrial neutrons and the lattice atoms, which may play an important role in the single event failure triggering mechanism in silicon carbide power devices.

Tests have also shown that the threshold voltage for SEF is much higher in SiC than in Si devices, e.g. some SiC MOSFETs exhibit higher LET rates only above their rated voltage [7]. In general silicon carbide devices display overall a better SEF resistance than silicon devices. Whether in silicon carbide MOSFETs with lower voltages a parasitic bipolar turn on effects, as in silicon, exists is unclear. Some of the tested SiC MOSFETs types have also shown gate rupture-like failures [7].

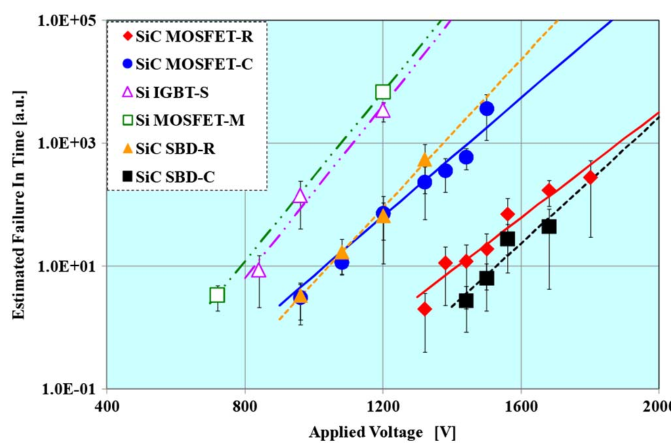

Fig. 4. Applied voltage dependent Estimated FIT of irradiated test samples with 1200V Voltage rating. Irradiated with the spallation neutron beam course at RCNP [7]

B. Heavy Ion radiation

Irradiation tests with heavy ions have shown that SiC MOSFETs have a rather low tolerance for heavy ion radiation damage. The determining factor here seems to be the increasing in gate leakage and subsequent gate rupture as well as the occurrence of ion induced streamers that short the device [1]. For the streamer-like failure, as with neutron radiation, a certain threshold voltage has to be reached, but now the threshold voltage is also dependent on the type of ion [9]. The higher the ion mass, the lower the needed threshold voltage for the occurrence of SEF [9]. To improve the heavy ion radiation robustness, e.g Al_2O_3 can be used as gate oxide [14] and devices with higher voltage ratings can be used.

IV. Discussion

All in all, silicon carbide seems to be a favorable material to produce more radiation resistant power devices. Partly because of the intrinsic properties of silicon carbide, as a wide band gap semiconductor, and the current fabrication processes that generate rather radiation resistant gate oxides in relation to their thickness, compared to silicon. The higher ionizing radiation robustness arises from the more resilient gate oxide, but also from the fact that the oxide/SiC interface generate less problematic interface states when subjected to ionizing radiation than the oxide/Si one. Also the neutron radiation response is better as seen in a higher FIT threshold voltage and a lower increase in FIT value as the applied voltage rises. This is possibly caused by the higher critical electric field strength of silicon carbide and the actual higher breakdown voltages of SiC MOSFETs compared to similar rated Si devices. Charged particle radiation can also be used in the manufacturing process to tweak and improve certain electrical properties. Why the robustness against heavy ion radiation is rather low is not fully known, except that the SiO_2 gate oxide is rather sensitive to heavy ion radiation. Al_2O_3 for example is noticeably less sensitive to heavy ion radiation as well as neutron and ionizing radiation. The formation of the gate oxide is the most important manufacturing step with regard to radiation hardness. For example nitrated gate oxides trap significantly more positive charge than non-nitrated ones. Optimization of the device structure for increased radiation hardness is also a good candidate, as the commercially available devices are not intentionally radiation hardened. If even more radiation hard devices are needed, SiC MESFETs and especially SiC BJT may be better suited.

V. Conclusion

This all seems to indicate that SiC MOSFETs are significantly more radiation resistant then Si devices, except in some cases for single event failures caused by heavy ion radiation. Current fabrication processes for SiC create quite radiation robust gate oxides [6]. It can be even further improved by using thinner gate oxides, non-nitrided SiO_2 gate oxides [10] or better yet, more radhard gate oxides like Al_2O_3, which also improve the heavy ion radiation robustness [14].

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